NEC

MOS INTEGRATED CIRCUIT

μPD30121

VR4121™
64-/32-BIT MICROPROCESSOR

DESCRIPTION

The μPD30121 (VR4121) is one of NEC's VR Series™ RISC (Reduced Instruction Set Computer) microprocessors and is a high-performance 64-/32-bit microprocessor employing the MIPS™ RISC architecture.

The VR4121 uses the high-performance, super power-saving VR4120™ as the CPU core, and has many peripheral functions such as a DMA controller, software modem interface, serial interface, keyboard interface, IrDA interface, touch panel interface, real-time clock, A/D converter, and D/A converter. Configured with these functions, the VR4121 is suitable for high-speed battery-driven portable information systems. The external memory bus width can be selected from 32 bits and 16 bits, realizing high-speed data transfer.

Detailed function descriptions are provided in the following user's manual. Be sure to read it before designing.

- **VR4121 User's Manual (U13569E)**

FEATURES

- Employs 64-bit MIPS architecture
  - Conforms to MIPS III instruction set (deleting FPU, LL, LLD, SC, and SCD instructions)
  - Optimized 6-stage pipeline
- Supports MIPS16 instruction set
- Supports high-speed product-sum operation instructions
- Supports four types of operating modes, enabling more effective power-consumption management
- Internal maximum operating frequency: 131/168 MHz
- On-chip clock generator
- Address space physical: 32 bits
  virtual: 40 bits
  Integrates 32 double entry TLBs
- High-capacity instruction/data separated cache memories
  Instruction: 16 Kbytes
  Data: 8 Kbytes
- Memory controller (ROM, EDO-type DRAM, synchronous DRAM (SDRAM), synchronous ROM (SROM), and flash memory supported)
- Keyboard interface and touch panel interface
- 4-channel DMA controller
- Serial interface (NS16550 compatible)
- IrDA interface for infrared communication
- Software modem interface
- A/D and D/A converters to support digital voice I/O
- Supports ISA bus subset
- Power supply voltage: $V_{DD}2$ = 2.5 V (internal), $V_{DD}3$ = 3.3 V (external) (131 MHz model)
- Package: 224-pin fine-pitch FBGA

APPLICATIONS

- Battery-driven portable information systems
- Embedded controllers, etc.

ORDERING INFORMATION

Part Number	Package	Internal Maximum Operating Frequency
μPD30121F1-131-GA1	224-pin plastic FBGA (16 × 16)	131 MHz
μPD30121F1-168-GA1	224-pin plastic FBGA (16 × 16)	168 MHz

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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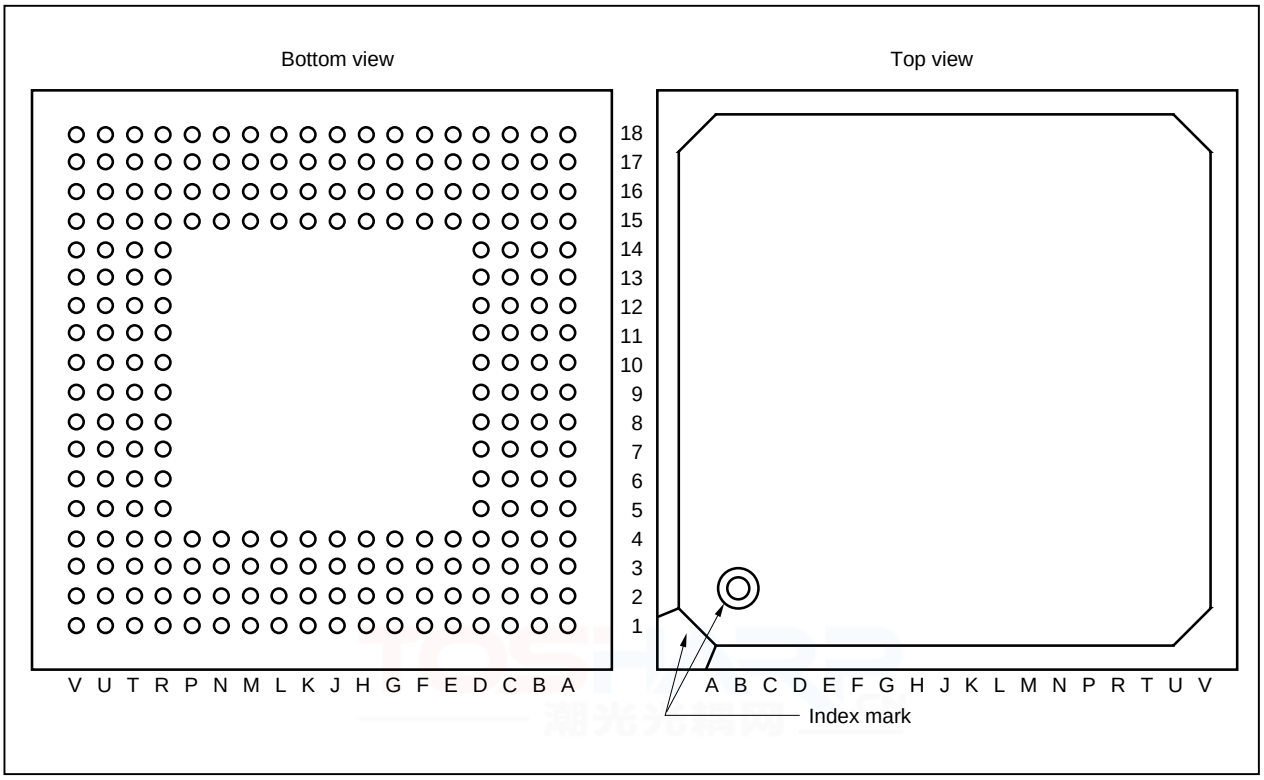
PIN CONFIGURATION

- 224-pin plastic FBGA (16 × 16)
  μPD30121F1-131-GA1
  μPD30121F1-168-GA1



Pin No.	Power Supply	Pin Name	Pin No.	Power Supply	Pin Name	Pin No.	Power Supply	Pin Name
A1	3.3 V	$V_{DD}3$	C15	3.3 V	RTS#/CLKSEL1	H15	3.3 V	GND3
A2	3.3 V	SHB#	C16	3.3 V	GND3	H16	3.3 V	KPORT6
A3	3.3 V	BUSCLK	C17	3.3 V	ILCSENSE	H17	3.3 V	KPORT4
A4	3.3 V	HLDACK#	C18	3.3 V	AFERST#	H18	2.5 V	$V_{DD}2$
A5	3.3 V	IOCHRDY	D1	3.3 V	DATA5	J1	3.3 V	DATA20/GPIO20
A6	3.3 V	MEMW#	D2	3.3 V	DATA3	J2	3.3 V	DATA17/GPIO17
A7	3.3 V	ADD23	D3	3.3 V	DATA6	J3	3.3 V	DATA22/GPIO22
A8	3.3 V	$V_{DD}3$	D4	3.3 V	GND3	J4	3.3 V	DATA19/GPIO19
A9	3.3 V	ADD18	D5	3.3 V	MEMCS16#	J15	3.3 V	KSCAN9/GPIO41
A10	3.3 V	ADD15	D6	3.3 V	ADD25/SCLK	J16	3.3 V	$V_{DD}3$
A11	3.3 V	ADD8	D7	3.3 V	GND3	J17	2.5 V	GND2
A12	3.3 V	ADD7	D8	3.3 V	ADD19	J18	3.3 V	KSCAN11/GPIO43
A13	2.5 V	$V_{DD}2$	D9	3.3 V	ADD16	K1	3.3 V	DATA23/GPIO23
A14	3.3 V	DCD#/GPIO15	D10	3.3 V	ADD14	K2	3.3 V	DATA26/GPIO26
A15	3.3 V	TXD/CLKSEL2	D11	3.3 V	$V_{DD}3$	K3	3.3 V	DATA25/GPIO25
A16	3.3 V	IRDOUT#	D12	3.3 V	GND3	K4	3.3 V	DATA21/GPIO21
A17	3.3 V	IRING	D13	3.3 V	ADD4	K15	3.3 V	KSCAN7/GPIO39
A18	3.3 V	$V_{DD}3$	D14	3.3 V	CTS#	K16	3.3 V	KSCAN10/GPIO42
B1	3.3 V	DATA1	D15	3.3 V	GND3	K17	3.3 V	KSCAN5/GPIO37
B2	3.3 V	IOR#	D16	3.3 V	GND3	K18	3.3 V	KSCAN8/GPIO40
B3	3.3 V	IOW#	D17	3.3 V	SDI	L1	3.3 V	DATA27/GPIO27
B4	3.3 V	LEDOUT#	D18	3.3 V	SDO	L2	3.3 V	DATA31/GPIO31
B5	3.3 V	FIRCLK	E1	3.3 V	DATA9	L3	3.3 V	DATA29/GPIO29
B6	3.3 V	HLDRQ#	E2	3.3 V	DATA4	L4	3.3 V	DATA24/GPIO24
B7	3.3 V	ZWS#	E3	3.3 V	DATA7	L15	3.3 V	KSCAN3/GPIO35
B8	3.3 V	ADD24	E4	3.3 V	DATA10	L16	3.3 V	KSCAN6/GPIO38
B9	3.3 V	ADD21	E15	3.3 V	OPD#	L17	3.3 V	KSCAN0/GPIO32
B10	3.3 V	ADD12	E16	3.3 V	HSPSCLK	L18	3.3 V	KSCAN4/GPIO36
B11	3.3 V	ADD6	E17	3.3 V	FS	M1	3.3 V	DATA30/GPIO30
B12	2.5 V	GND2	E18	3.3 V	HC0	M2	3.3 V	$V_{DD}3$
B13	3.3 V	DSR#	F1	3.3 V	DATA13	M3	3.3 V	GND3
B14	3.3 V	IRDIN	F2	3.3 V	DATA8	M4	3.3 V	DATA28/GPIO28
B15	3.3 V	FIRDIN#/SEL	F3	3.3 V	DATA11	M15	3.3 V	KSCAN2/GPIO34
B16	3.3 V	BATTINH/BATTINT#	F4	3.3 V	DATA14	M16	3.3 V	MIPS16EN
B17	3.3 V	OFFHOOK	F15	3.3 V	KPORT3	M17	3.3 V	GND3
B18	3.3 V	MUTE	F16	3.3 V	HSPMCLK	M18	3.3 V	KSCAN1/GPIO33
C1	3.3 V	DATA2	F17	3.3 V	TELCON	N1	2.5 V	$V_{DD}2$
C2	3.3 V	DATA0	F18	3.3 V	KPORT1	N2	3.3 V	ADD3
C3	3.3 V	SMODE2	G1	2.5 V	$V_{DD}2$	N3	3.3 V	ADD10
C4	3.3 V	CKE	G2	3.3 V	DATA12	N4	3.3 V	GND2
C5	3.3 V	GND3	G3	3.3 V	DATA15	N15	3.3 V	GND3
C6	3.3 V	IOCS16#	G4	3.3 V	GND3	N16	3.3 V	$V_{DD}3$
C7	3.3 V	MEMR#	G15	3.3 V	KPORT7	N17	2.5 V	$V_{DD}P$
C8	3.3 V	ADD22	G16	3.3 V	KPORT2	N18	3.3 V	GND3
C9	3.3 V	ADD20	G17	3.3 V	KPORT0	P1	3.3 V	ADD9
C10	3.3 V	ADD17	G18	3.3 V	KPORT5	P2	3.3 V	ADD0
C11	3.3 V	ADD13	H1	3.3 V	DATA16/GPIO16	P3	3.3 V	ADD2
C12	3.3 V	ADD5	H2	2.5 V	GND2	P4	3.3 V	ADD11
C13	3.3 V	R_XD	H3	3.3 V	DATA18/GPIO18	P15	2.5 V	$V_{DD}2$ ($V_{DD}PD$)
C14	3.3 V	DTR#/CLKSEL0	H4	3.3 V	$V_{DD}3$	P16	2.5 V	GNDP

Remark # indicates active low.

Pin No.	Power Supply	Pin Name	Pin No.	Power Supply	Pin Name	Pin No.	Power Supply	Pin Name
P17	3.3 V	CLKX2	T6	3.3 V	AV_{DD}	U13	3.3 V	GPIO9
P18	2.5 V	GND2 (GNDPD)	T7	3.3 V	LCAS#	U14	3.3 V	SYSDIR/GPIO6
R1	3.3 V	ADD1	T8	3.3 V	ROMCS2#	U15	3.3 V	SCAS#/GPIO5
R2	3.3 V	POWER	T9	3.3 V	RD#	U16	3.3 V	GPIO1
R3	3.3 V	GND3	T10	3.3 V	WR#	U17	3.3 V	GPIO2
R4	3.3 V	GND3	T11	3.3 V	DBUS32/GPIO48	U18	3.3 V	CGND
R5	3.3 V	AUDIOIN	T12	3.3 V	DDOUT/GPIO44	V1	3.3 V	$V_{DD}3$
R6	3.3 V	DV_{DD}	T13	3.3 V	GPIO11	V2	3.3 V	PIUGND
R7	3.3 V	MRAS2#/ULCAS#	T14	3.3 V	GPIO8	V3	3.3 V	TPX0
R8	3.3 V	MRAS1#	T15	3.3 V	GND3	V4	3.3 V	TPY1
R9	3.3 V	ROMCS1#	T16	3.3 V	GND3	V5	3.3 V	ADIN2
R10	3.3 V	RSTOUT	T17	3.3 V	GPIO0	V6	3.3 V	AUDIOOUT
R11	3.3 V	GND3	T18	3.3 V	RTCX1	V7	3.3 V	MRAS3#/UUCAS#
R12	3.3 V	SMODE1/GPIO49	U1	3.3 V	MPOWER	V8	3.3 V	MRAS0#
R13	3.3 V	DDIN/GPIO45	U2	3.3 V	RTCRST#	V9	3.3 V	ROMCS0#
R14	3.3 V	GPIO12	U3	3.3 V	AGND	V10	3.3 V	$V_{DD}3$
R15	3.3 V	GND3	U4	3.3 V	TPX1	V11	3.3 V	LCDCS#
R16	3.3 V	CV_{DD}	U5	3.3 V	TPY0	V12	3.3 V	DCTS#/GPIO47
R17	3.3 V	RTCX2	U6	3.3 V	ADIN1	V13	3.3 V	GPIO14
R18	3.3 V	CLKX1	U7	3.3 V	DGND	V14	3.3 V	GPIO10
T1	3.3 V	POWERON	U8	3.3 V	UCAS#	V15	3.3 V	SPOWER/GPIO7
T2	3.3 V	RSTSW#	U9	3.3 V	ROMCS3#	V16	3.3 V	SRAS#/GPIO4
T3	3.3 V	GND3	U10	3.3 V	LDCRDY	V17	3.3 V	GPIO3
T4	3.3 V	$PIUV_{DD}$	U11	3.3 V	DRTS#/GPIO46	V18	3.3 V	$V_{DD}3$
T5	3.3 V	ADIN0	U12	3.3 V	GPIO13			

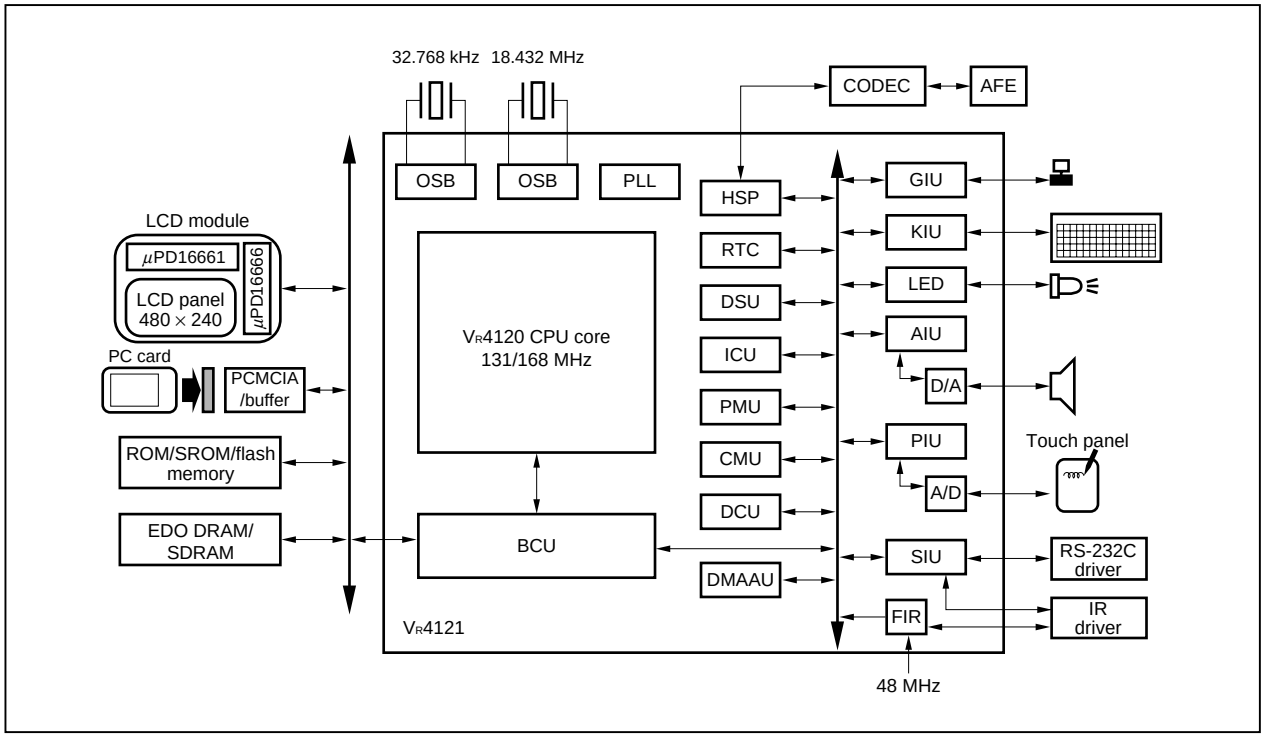
Remark # indicates active low.

PIN IDENTIFICATION

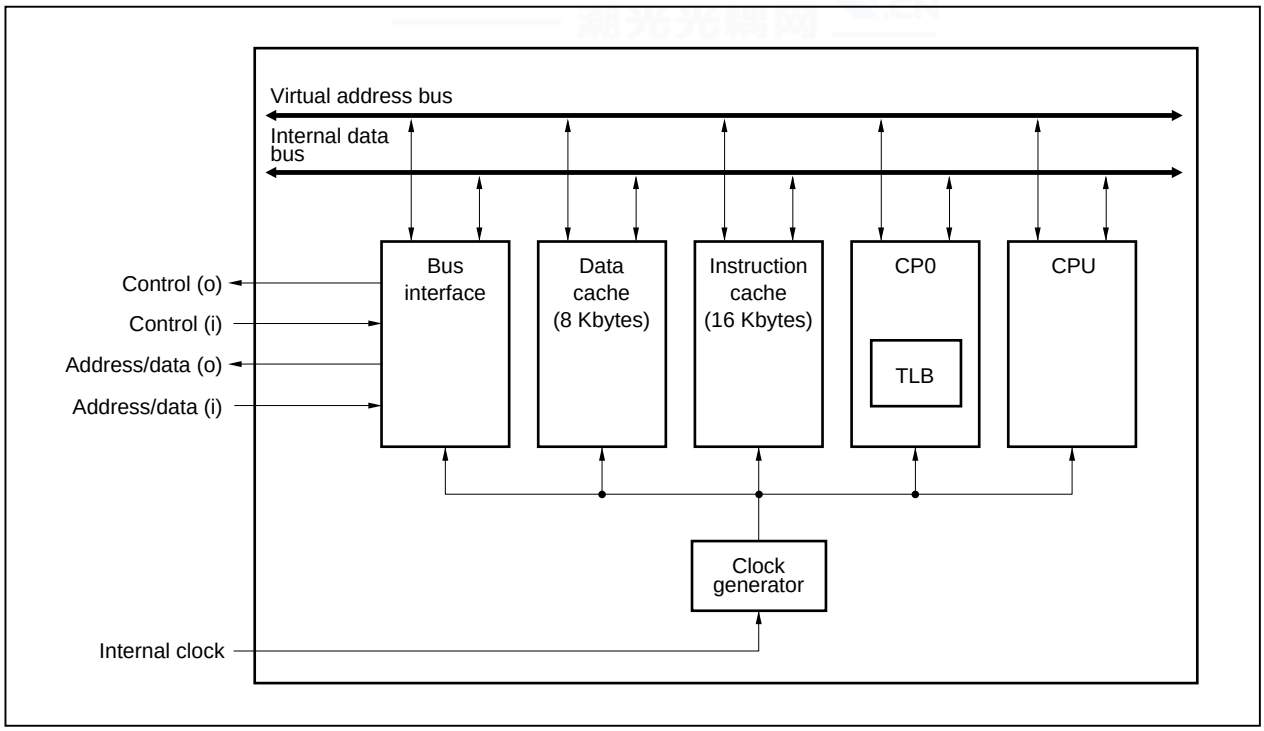
ADD (0:25):	Address Bus
ADIN (0:2):	General Purpose Input for A/D
AFERST#:	AFE Reset
AGND:	GND for A/D
AUDIOIN:	Audio Input
AUDIOOUT:	Audio Output
AV_{DD}:	V_{DD} for A/D
BATTINH:	Battery Inhibit
BATTINT#:	Battery Interrupt Request
BUSCLK:	System Bus Clock
CGND:	GND for Oscillator
CKE:	Clock Enable
CLKSEL (0:2):	Clock Select
CLKX1:	Clock X1
CLKX2:	Clock X2
CTS#:	Clear to Send
CV_{DD}:	V_{DD} for Oscillator
DATA (0:31):	Data Bus
DBUS32:	Data Bus 32
DCD#:	Data Carrier Detect
DCTS#:	Debug Serial Clear to Send
DDIN:	Debug Serial Data Input
DDOUT:	Debug Serial Data Output
DGND:	GND for D/A
DRTS#:	Debug Serial Request to Send
DSR#:	Data Set Ready
DTR#:	Data Terminal Ready
DV_{DD}:	V_{DD} for D/A
FIRCLK:	FIR Clock
FIRDIN#:	FIR Data Input
FS:	Frame Synchronization
GND2, GND3:	Ground
GNDP, GNDPD:	Ground for PLL
GPIO (0:49):	General Purpose I/O
HC0:	Hardware Control 0
HLDACK#:	Hold Acknowledge
HLDRQ#:	Hold Request
HSPMCLK:	HSP Codec Master Clock
HSPSCLK:	HSP Codec Serial Clock
ILCSENSE:	Input Loop Current Sensing
IOCHRDY:	I/O Channel Ready
IOCS16#:	I/O Chip Select 16
IOR#:	I/O Read
IOW#:	I/O Write
IRDIN:	IrDA Data Input
IRDOUT#:	IrDA Data Output
IRING:	Input Ring
KPORT (0:7):	Key Code Data Input
KSCAN (0:11):	Key Scan Line
LCAS#:	Lower Column Address Strobe
LCDCS#:	LCD Chip Select
LCDRDY:	LCD Ready
LEDOUT#:	LED Output
MEMCS16#:	Memory Chip Select 16
MEMR#:	Memory Read
MEMW#:	Memory Write
MIPS16EN:	MIPS16 Enable
MPOWER:	Main Power
MRAS(0:3)#:	DRAM Row Address Strobe
MUTE:	Mute
OFFHOOK:	Off Hook
OPD#:	Output Power Down
PIUGND:	GND for Touch Panel Interface
$PIUV_{DD}$:	V_{DD} for Touch Panel Interface
POWER:	Power Switch
POWERON:	Power On State
RD#:	Read
ROMCS(0:3)#:	ROM Chip Select
RSTOUT:	System Bus Reset Output
RSTSW#:	Reset Switch
RTCRST#:	Real-time Clock Reset
RTCX1:	Real-time Clock X1
RTCX2:	Real-time Clock X2
RTS#:	Request to Send
RxD:	Receive Data
SCAS#:	Column Address Strobe for SDRAM/SROM
SCLK:	SDRAM/SROM Clock
SDI:	HSP Serial Data Input
SDO:	HSP Serial Data Output
SEL:	IrDA Module Select
SHB#:	System Hi-Byte Enable
SMODE (1:2):	SDRAM Mode
SPOWER:	SDRAM Power Control
SRAS#:	Row Address Strobe for SDRAM/SROM
SYSDIR:	System Bus Buffer Direction
TELCON:	Telephone Control
TPX (0:1):	Touch Panel X I/O
TPY (0:1):	Touch Panel Y I/O
TxD:	Transmit Data
UCAS#:	Upper Column Address Strobe
ULCAS#:	Lower Byte of Upper Column Address Strobe
UUCAS#:	Upper Byte of Upper Column Address Strobe
$V_{DD}2$, $V_{DD}3$:	Power Supply Voltage
$V_{DD}P$, $V_{DD}PD$:	V_{DD} for PLL
WR#:	Write
ZWS#:	Zero Wait State

Remark # indicates active low.

INTERNAL BLOCK DIAGRAM AND EXAMPLE OF CONNECTION OF EXTERNAL BLOCKS



CPU CORE INTERNAL BLOCK DIAGRAM



CONTENTS

1. PIN FUNCTIONS

Remark # indicates active low.

1.1 Pin Functions

(1) System bus interface signals

(1/3)

Signal	I/O	Function
ADD25/SCLK	O	This function differs depending on how the SMODE (1:2) signal is set. <When SMODE (1:2) signal = 00> This is a 25-bit address bus. <When SMODE (1:2) signal ≠ 00> This is the operating clock for SDRAM and SROM.
ADD (0:24)	O	This is a 25-bit address bus. The VR4121 uses this to specify addresses for the SDRAM, SROM, DRAM, ROM, LCD, or system bus (ISA).
DATA (0:15)	I/O	This is a 16-bit data bus. The VR4121 uses this to transmit and receive data with a SDRAM, SROM, DRAM, ROM, LCD, or system bus.
DATA (16:31)/ GPIO (16:31)	I/O	This function differs depending on how the DBUS32 signal is set. <When DBUS32 signal = 1> This is the high-order 16 bits of the 32-bit data bus. This bus is used for transmitting and receiving data between the VR4121 and the DRAM and ROM. <When DBUS32 signal = 0> This is a general-purpose I/O port.
LCDCS#	O	This is the LCD chip select signal. This signal is active when the VR4121 is performing LCD access and high-speed system bus access using the ADD/DATA bus.
RD#	O	This is active when the VR4121 is reading data from the LCD, SDRAM, SROM, DRAM, or ROM.
WR#	O	This is active when the VR4121 is writing data to the LCD, SDRAM, or DRAM.
LCDRDY	I	This is the LCD ready signal. Set this signal as active when the LCD controller is ready to receive access from the VR4121.
ROMCS (2:3)#	O	The function differs with the setting of the DBUS32 signal. <When DBUS32 signal = 1> This becomes the chip select signal for the extended ROM, SROM, DRAM, or SDRAM. <When DBUS32 signal = 0> This is the ROM or SROM chip select signal.
ROMCS (0:1)#	O	This is the ROM or SROM chip select signal.
CKE	O	This is the SDRAM or SROM clock enable signal. When using neither SDRAM nor SROM, connect to GND or leave open.
UUCAS#/ MRAS3#	O	This function differs depending on how the DBUS32 signal is set or types of memory to be accessed. <When DBUS32 signal = 1> When accessing DRAM (EDO type): This signal is active (UUCAS#) when a valid column address is output via the ADD bus during access of DATA (24:31) in the 32-bit data bus. When accessing SDRAM: This is the I/O buffer control signal (UUDQM#) that is used during access of DATA (24:31) signal in the 32 bit data bus. During 32-bit access of LCD/high-speed system memory: Byte enable signal that is used during access of DATA (24:31) signal. <When DBUS32 signal = 0> When accessing DRAM (EDO type): This is the DRAM's RAS signal (MRAS3#). This signal is active when a valid row address is output via the ADD bus for the DRAM connected to the high-order address. When accessing SDRAM: This is the SDRAM's chip select signal (CS3#). This signal is active when a command is issued for the SDRAM connected to the high-order address.

(2/3)

Signal	I/O	Function
ULCAS#/ MRAS2#	O	This function differs depending on how the DBUS32 signal is set and type of memory being accessed. <When DBUS32 signal = 1> When accessing DRAM (EDO type): This signal is active (ULCAS#) when a valid column address is output via the ADD bus during access of DATA (16:23) signal in the 32-bit data bus. When accessing SRAM: This is the I/O buffer control signal (ULDQM#) that is used during access of DATA (16:23) signal in the 32-bit data bus. During 32-bit access of LCD/high-speed system memory: Byte enable signal that is used during access of DATA (16:23) signal. <When DBUS32 signal = 0> When accessing DRAM (EDO type): This is the DRAM's RAS signal (MRAS2#). This signal is active when a valid row address is output via the ADD bus for the DRAM connected to the next highest address after the highest high-order address. When accessing SDRAM: This is the SDRAM's chip select signal (CS2#). This signal is active when a command is issued for the SDRAM connected to the second highest high-order address.
MRAS (0:1)#	O	This function differs depending on the type of memory being accessed. <When accessing DRAM (EDO type)> This is the DRAM's RAS-only signal. <When accessing SDRAM> This is the SDRAM's chip select signal (CS (0:1)#).
UCAS#	O	This function differs depending on the type of memory being accessed. <When accessing DRAM (EDO type)> This is the DRAM's CAS signal. This signal is active when a valid column address is output via the ADD bus during access of DATA (8:15) signal in the DRAM. <When accessing SDRAM> This is the I/O buffer control signal (UDQM#) that is used during access of DATA (8:15) signal. < During 32-bit access of LCD/high-speed system memory > This is the byte enable signal that is used during access of DATA (8:15) signal. This signal is active when a valid address is output via the ADD bus for access to DATA (8:15) signal when the size of the access bus to the LCD is 32 bits.
LCAS#	O	This function differs depending on the type of memory being accessed. <When accessing DRAM (EDO type)> This is the DRAM's CAS signal. This signal is active when a valid column address is output via the ADD bus during access of DATA (0:7) signal in the DRAM. <When accessing SDRAM> This is the I/O buffer control signal (LDQM#) that is used during access of DATA (0:7) signal. < During 32-bit access of LCD/high-speed system memory > This is the byte enable signal that is used during access of DATA (0:7) signal.
BUSCLK	O	This is the system bus clock. It is used to output the clock that is supplied to the controller on the system bus. Its frequency is determined based on the status of the CLKSEL (0:2) signal. Ordinarily, the frequency is 1/4 of the TClock frequency. (See **(5) RS-232C interface signals**). The frequency can be changed via the PMU register settings.
SHB#	O	This is the system bus high-byte enable signal. During 16-bit system bus access, this signal is active when the high-order byte is valid on the data bus.
IOR#	O	This is the system bus I/O read signal. It is active when the VR4121 accesses the system bus to read data from an I/O port.
IOW#	O	This is the system bus I/O write signal. It is active when the VR4121 accesses the system bus to write data to an I/O port.
MEMR#	O	This is the system bus memory read signal. It is active when the VR4121 accesses the system bus to read data from memory.
MEMW#	O	This is the system bus memory write signal. It is active when the VR4121 accesses the system bus to write data to memory.
ZWS#	I	This is the system bus zero wait state signal. Set this signal as active to enable the controller on the system bus to be accessed by the VR4121 without a wait interval.

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Signal	I/O	Function
RSTOUT	O	This is the system bus reset signal. It is active when the VR4121 resets the system bus controller (during bus timeout, manipulation of BCUCNTREG1 register, and power-down mode).
MEMCS16#	I	This is a dynamic bus sizing request signal. Set this signal as active when system bus memory accesses data in 16-bit width. This signal is invalid when 32-bit width is selected using LCD/high-speed system bus.
IOCS16#	I	This is a dynamic bus sizing request signal. Set this signal as active when system bus I/O accesses data in 16-bit width. This signal is invalid when 32-bit width is selected using LCD/high-speed system bus.
IOCHRDY	I	This is the system bus ready signal. Set this signal as active when the system bus controller is ready to be accessed by the VR4121.
HLDRQ#	I	This is a hold request signal for the system bus and DRAM bus that is sent from an external bus master.
HLDACK#	O	This is a hold acknowledge signal for the system bus and DRAM bus that is sent to an external bus master.
SRAS#/GPIO4	I/O	This function differs depending on the type of memory being accessed. <When accessing DRAM (EDO type)> This is a general-purpose I/O port. <When accessing SDRAM> This is the RAS signal for SDRAM and SROM only.
SCAS#/GPIO5	I/O	This function differs depending on the type of memory being accessed. <When accessing DRAM (EDO type)> This is a general-purpose I/O port. <When accessing SDRAM> This is the CAS signal for SDRAM and SROM only.
SYSDIR/GPIO6	I/O	This function differs depending on the type of memory being accessed. <When accessing DRAM (EDO type)> This is a general-purpose I/O port. <When accessing SDRAM> This is the direction control signal for the buffer used to reduce the DATA bus's load.
SPOWER/ GPIO7	I/O	This function differs depending on the type of memory being accessed. <When accessing DRAM (EDO type)> This is a general-purpose I/O port. <When accessing SDRAM> This is the SDRAM's power supply control signal.

(2) Clock interface signals

Signal	I/O	Function
RTCX1	I	This is the 32.768-kHz oscillator's input pin. It is connected to one side of a crystal resonator.
RTCX2	O	This is the 32.768-kHz oscillator's output pin. It is connected to one side of a crystal resonator.
CLKX1	I	This is the 18.432-MHz oscillator's input pin. It is connected to one side of a crystal resonator.
CLKX2	O	This is the 18.432-MHz oscillator's output pin. It is connected to one side of a crystal resonator.
FIRCLK	I	This is the 48-MHz clock input pin. Fix this at high level when FIR is not used.

(3) Battery monitor interface signals

Signal	I/O	Function
BATTINH/ BATTINT#	I	This function differs depending on how the MPOWER signal is set. <When MPOWER signal = 0> BATTINH function This signal enables/prohibits activation due to power-on. 1 : Enable activation 0 : Prohibit activation <When MPOWER signal = 1> BATTINT# function This is an interrupt signal that is output when remaining power is low during normal operations. The external agent checks the remaining battery power. Activate the signal at this pin if voltage sufficient for operations cannot be supplied.

(4) Initialization interface signals

Signal	I/O	Function
MPOWER	O	This signal indicates the VR4121 is operating. This signal is inactive during Hibernate mode.
POWERON	O	This signal indicates the VR4121 is ready to operate. It becomes active when a power-on factor is detected and becomes inactive when the BATTINH/BATTINT# signal check operation is completed.
POWER	I	This is a VR4121 activation signal.
RSTSW#	I	This is a VR4121 reset signal.
RTCRST#	I	This signal resets RTC. When power is first supplied to a device, the external agent must assert the signal at this pin for about 2 s.

(5) RS-232C interface signals

Signal	I/O	Function
RxD	I	This is a receive data signal. It is used when the RS-232C controller sends serial data to the VR4121.
CTS#	I	This is a transmit enable signal. Assert this signal when the RS-232C controller is ready to receive transmission of serial data.
DCD#/ GPIO15	I	This is a carrier detection signal. Assert this signal when valid serial data is being received. It is also used when detecting a power-on factor for the VR4121. When this pin is not used for DCD# signal, this pin can be used as an interrupt detection function for the GIU unit.
DSR#	I	This is the data set ready signal. Assert this signal when the RS-232C controller is ready to receive/transmit serial data between the controller and the VR4121.
TxD/ CLKSEL2, RTS#/ CLKSEL1, DTR#/ CLKSEL0	I/O	This function differs depending on the operating status. <During normal operation (output)> Signals used for serial communication TxD signal : This is a transmit data signal. It is used when the VR4121 sends serial data to the RS-232C controller. RTS# signal : This is a transmit request signal. This signal is asserted when the VR4121 is ready to receive serial data from the RS-232C controller. DTR# signal : This is a terminal equipment ready signal. This signal is asserted when the VR4121 is ready to transmit or receive serial data. <When RTC reset (input)> Signals (CLKSEL (2:0) signal) used to set the CPU core operation frequency, BUSCLK signal frequency, and internal bus clock frequency. These signals are sampled when the RTCRST# signal changes from low level to high level. The relationships between the CLKSEL (2:0) signal setting and each clock frequency are shown below.

CLKSEL (2:0) signal	CPU core operation frequency (PClock)	SDRAM/SROM operation frequency (VTClock) MIN.	SDRAM/SROM operation frequency (VTClock) MAX.	BUSCLK signal frequency (When TClock output)	BUSCLK signal requency (When 1/4 of TClock)	Interrupt control clock frequency (MasterOut)
111[Note 1]	RFU	RFU	RFU	RFU	RFU	RFU
110[Note 2]	168.5 MHz	28.1 MHz	56.2 MHz	28.1 MHz	7.0 MHz	7.0 MHz
101[Note 2]	147.5 MHz	29.5 MHz	59.0 MHz	29.5 MHz	7.4 MHz	7.4 MHz
100	131.1 MHz	32.8 MHz	65.5 MHz	32.8 MHz	8.2 MHz	8.2 MHz
011	118.0 MHz	29.5 MHz	59.0 MHz	29.5 MHz	7.4 MHz	7.4 MHz
010	98.3 MHz	32.8 MHz	65.5 MHz	32.8 MHz	8.2 MHz	8.2 MHz
001	90.7 MHz	30.2 MHz	60.5 MHz	30.2 MHz	7.6 MHz	7.6 MHz
000	78.6 MHz	26.2 MHz	52.4 MHz	26.2 MHz	6.6 MHz	6.6 MHz

Notes 1. Do not set CLKSEL (2:0) = 111.

2. The settings CLKSEL (2:0) = 110 and 101 are only guaranteed for the 168 MHz model. Do not apply these settings to the 131 MHz model.

(6) IrDA interface signals

Signal	I/O	Function
IRDIN	I	This is an IrDA serial data input signal. It is used when the VR4121 sends serial data to the IrDA controller, for both FIR and SIR. If the IrDA controller used is an HP product, however, this signal should be used for only SIR.
FIRDIN#/SEL	I/O	This function differs according to the IrDA controller used. <HP's controller> FIRDIN#: It is an FIR receive data input signal. <TEMIC's controller> SEL: It is an output port for external FIR/SIR switching. <SHARP's controller> Use is prohibited.
IRDOUT#	O	This is the IrDA serial data output signal. It is used when the IrDA controller sends serial data from the VR4121.

(7) Debug serial interface signals

Signal	I/O	Function
DDOUT/ GPIO44	O	This is the debug serial data output signal. It is used when the VR4121 sends serial data to an external debug serial controller. When this pin is not used for the DDOUT signal, it can be used as a general-purpose output port.
DDIN/ GPIO45	I/O	This is the debug serial data input signal. It is used when an external debug serial data controller sends serial data to the VR4121. When this pin is not used for the DDIN signal, it can be used as a general-purpose output port.
DRTS#/ GPIO46	O	This is a transmission request signal. The VR4121 asserts this signal before sending serial data. When this pin is not used for the DRTS# signal, it can be used as a general-purpose output port.
DCTS#/ GPIO47	I/O	This is a transmit acknowledge signal. The VR4121 asserts this signal when it is ready to receive transmitted serial data. When this pin is not used for the DCTS# signal, it can be used as a general-purpose output port.

(8) Keyboard interface signals

Signal	I/O	Function
KPORT (0:7)	I	This is a keyboard scan data input signal. It is used to scan for pressed keys on the keyboard.
KSCAN (0:11)/ GPIO (32:43)	O	These signal are used as keyboard scan data output signals and a general-purpose output port. The scan line is set as active when scanning for pressed keys on the keyboard. Signals that are not used for KSCAN signals can be used as a general-purpose output port.

(9) Audio interface signals

Signal	I/O	Function
AUDIOIN	I	This pin is the audio input signal.
AUDIOOUT	O	This is an audio output signal. Analog signals that have been converted via the on-chip 10-bit D/A converter are output.

(10) Touch panel/general purpose A/D interface signals

Signal	I/O	Function
TPX (0:1)	I/O	This is an I/O signal that is used for the touch panel. It uses the voltage applied to the X coordinate and the voltage input to the Y coordinate to detect which coordinates on the touch panel are being pressed.
TPY (0:1)	I/O	This is an I/O signal that is used for the touch panel. It uses the voltage applied to the Y coordinate and the voltage input to the X coordinate to detect which coordinates on the touch panel are being pressed.
ADIN (0:2)	I	This is a general-purpose A/D input signal.

(11) General-purpose I/O Signals

Signal	I/O	Function
GPIO (0:3)	I/O	These are maskable power-on factors. After start-up, they are used as ordinary general-purpose I/O ports.
GPIO4/SRAS#	I/O	See **(1) System bus interface signals**.
GPIO5/SCAS#	I/O	See **(1) System bus interface signals**.
GPIO6/SYSDIR	I/O	See **(1) System bus interface signals**.
GPIO7/SPOWER	I/O	See **(1) System bus interface signals**.
GPIO8	I/O	These are general-purpose I/O ports.
GPIO (9:12)	I/O	These are maskable power-on factors. After start-up, they are used as ordinary general-purpose I/O ports.
GPIO (13:14)	I/O	These are general-purpose I/O ports.
GPIO (16:31)/DATA (16:31)	I/O	See **(1) System bus interface signals**.
GPIO (32:43)/KSCAN (0:11)	O	See **(8) Keyboard interface signals**.
GPIO44/DDOUT	O	See **(7) Debug serial interface signals**.
GPIO45/DDIN	I/O	See **(7) Debug serial interface signals**.
GPIO46/DRTS#	O	See **(7) Debug serial interface signals**.
GPIO47/DCTS#	I/O	See **(7) Debug serial interface signals**.
GPIO48/DBUS32	I/O	See **(14) Initial setting signals**.
GPIO49/SMODE1	I/O	See **(14) Initial setting signals**.

(12) HSP MODEM interface signals

Signal	I/O	Function
IRING	I	RING signal detect signal. This pin becomes active when the RING signal is detected.
ILCSENSE	I	Handset detect signal
OFFHOOK	O	On-hook relay control signal
MUTE	O	Modem speaker mute control signal
AFERST#	O	CODEC reset signal
SDI	I	Serial input signal from CODEC
FS	I	Frame synchronization signal from CODEC
SDO	O	Serial output signal to CODEC
HSPSCLK	I	Operation clock input of modem interface block for CODEC
TELCON	O	Handset relay control signal
HC0	O	CODEC control signal
HSPMCLK	O	Clock output to CODEC
OPD#	O	Use this pin for controlling power of CODEC and DAA. This signal is set as active when the power supply of CODEC and DAA is ON.

(13) LED interface signal

Signal	I/O	Function
LEDOUT#	O	This is an output signal for lighting LEDs.

(14) Initial setting signals

Signal Name	I/O	Function
DBUS32/ GPIO48	I/O	The function differs depending on the operating status. <During normal operation (output)> This can be used as a general-purpose output port. <After an RTC reset (input)> This is the switching signal for the data bus width. This signal is sampled at 1RTC clock cycle after the RTCRST# signal changes from low level to high level. 1: The data bus has a 32-bit width. 0: The data bus has a 16-bit width.
SMODE1/ GPIO49	I/O	The function differs depending on the operating status. <During normal operation (output)> This can be used as a general-purpose output port. < After an RTC reset (input)> This is a switching signal for the memory being used. It is used in combination with the SMODE2 signal. This signal is sampled at 1RTC clock cycle after the RTCRST# signal changes from low level to high level.
SMODE2	I	This a switching signal for the memory being used. It is used in combination with the SMODE1 signal. This signal is sampled when the RTCRST# signal changes from low level to high level. The relation between the SMODE (2:1) signal and the memory being used is shown below. SMODE (2:1) signal — Used Memory 11 — ROM: SROM; RAM: SDRAM 10 — ROM: Flash memory, PageROM, ordinary ROM; RAM: SDRAM 01 — ROM (boot bank): Flash memory, PageROM, ordinary ROM; ROM (except boot bank): SROM; RAM: SDRAM 00 — ROM: Flash memory, PageROM, ordinary ROM; RAM: DRAM (EDO type)
MIPS16EN	I	This pin enables the use of MIPS16 instructions. This signal is sampled at 1RTC clock cycle after the RTCRST# signal changes from low level to high level. 1: Enables the use of MIPS16 instructions. 0: Disables the use of MIPS16 instructions.

(15) Dedicated V_{DD} and GND signals

Signal Name	Power-Supply System	Function
V_{DD}P	2.5 V	Dedicated V_{DD} for the PLL analog unit
GNDP	2.5 V	Dedicated GND for the PLL analog unit
V_{DD}PD	2.5 V	Dedicated V_{DD} for the PLL digital unit. Its function is identical to V_{DD}2.
GNDPD	2.5 V	Dedicated GND for the PLL digital unit. Its function is identical to GND2.
CV_{DD}	3.3 V	Dedicated V_{DD} for the oscillator
CGND	3.3 V	Dedicated GND for the oscillator
DV_{DD}	3.3 V	Dedicated V_{DD} for the D/A converter. The voltage applied to this pin becomes the maximum of the analog output of AUDIOOUT signal.
DGND	3.3 V	Dedicated GND for D/A converter. The voltage applied to this pin becomes the minimum of the analog output of AUDIOOUT signal.
AV_{DD}	3.3 V	Dedicated V_{DD} for the A/D converter. The voltage applied to this pin becomes the maximum voltage that can be detected by the A/D interface signals (8 lines).
AGND	3.3 V	Dedicated GND for the A/D converter. The voltage applied to this pin becomes the minimum voltage that can be detected by the A/D interface signals (8 lines).
$PIUV_{DD}$	3.3 V	Dedicated V_{DD} for touch-sensitive panel interface
PIUGND	3.3 V	Dedicated GND for touch-sensitive panel interface
V_{DD}2	2.5 V	Normal 2.5-V system V_{DD}
GND2	2.5 V	Normal 2.5-V system GND
V_{DD}3	3.3 V	Normal 3.3-V system V_{DD}
GND3	3.3 V	Normal 3.3-V system GND

Caution The V_R4121 has two types of power supplies. There are no restrictions as to the sequence in which these power supplies are applied. However, do not apply one type of power for more than one second while the other power supply is not applied.

1.2 Pin Status in Specific Status

(1/4)

Pin Name	After Reset by the RTC Reset	After Reset by the Deadman's Switch or RSTSW# Signal	In the Suspend Mode	In the Hibernate Mode or Shut Down by the HAL Timer	During a Bus Hold
ADD25/SCLK	0	**Note 1**	**Note 2**	0	Hi-Z
ADD (0:24)	0	0	**Note 2**	0	Hi-Z
DATA (0:15)	0	0	**Note 2**	0	Hi-Z
DATA (16:31)/ GPIO (16:31)	0/ Hi-Z	0/ Hi-Z	**Note 2**	0/ Hi-Z	Hi-Z/ **Note 2**
LCDCS#	Hi-Z	1	1	Hi-Z	1
RD#	Hi-Z	1	1	Hi-Z	Hi-Z
WR#	Hi-Z	1	1	Hi-Z	Hi-Z
LCDRDY	–	–	–	–	–
ROMCS (2:3)#	Hi-Z	**Note 3**	**Note 3**	**Note 3**	**Note 3**
ROMCS (0:1)#	Hi-Z	1	1	Hi-Z	1
UUCAS#/MRAS3#	**Note 4**	**Note 5**	**Note 6**	0	Hi-Z
ULCAS#/MRAS2#	**Note 4**	**Note 5**	**Note 6**	0	Hi-Z
MRAS (0:1)#	Hi-Z	1	1	1	Hi-Z
UCAS#	0	**Note 7**	0	0	Hi-Z
LCAS#	0	**Note 7**	0	0	Hi-Z
BUSCLK	0	0	**Note 2**	0	**Note 8**

Notes 1. This differs depending on the setting of the SCLK bit in the SDRAMMODEREG register.
When SCLK bit has a value of "1": outputs clock.
When SCLK bit has a value of "0": low level is output.

2. Maintains the state of the previous Full-speed Mode.

3. When used as the chip select for the ROM or extended ROM, this is the same as ROMCS (0:1)# pins.
When used as the RAS for the extended DRAM, this is the same as MRAS (0:1)# pins.

4. When DBUS32 signal = 1, this becomes the high impedance state.
When DBUS32 signal = 0, the high level is output.

5. When DBUS32 signal = 1: See **Note 7** below.
When DBUS32 signal = 0: high level is output.

6. When DBUS32 signal = 1: low level is output.
When DBUS32 signal = 0: high level is output.

7. Reset by the RSTSW# signal: The pin outputs a low level. (Self refresh)
Reset by the Deadman's switch: The pin outputs a high level.

8. Bus hold from the Suspend Mode: The state of the previous Full-speed Mode is maintained.
Bus hold from Full-speed Mode or Standby Mode: Outputs clocks.

Remark 0: low level, 1: high level, Hi-Z: high impedance

(2/4)

Pin Name	After Reset by the RTC Reset	After Reset by the Deadman's Switch or RSTSW# Signal	In the Suspend Mode	In the Hibernate Mode or Shut Down by the HAL Timer	During a Bus Hold
SHB#	Hi-Z	1	1	Hi-Z	Hi-Z
IOR#	Hi-Z	1	1	Hi-Z	Hi-Z
IOW#	Hi-Z	1	1	Hi-Z	Hi-Z
MEMR#	Hi-Z	1	1	Hi-Z	Hi-Z
MEMW#	Hi-Z	1	1	Hi-Z	Hi-Z
ZWS#	–	–	–	–	–
RSTOUT	Hi-Z	1	0	Hi-Z	**Note 1**
IOCS16#	–	–	–	–	–
MEMCS16#	–	–	–	–	–
IOCHRDY	–	–	–	–	–
HLDRQ#	–	–	–	–	–
HLDACK#	Hi-Z	1	**Note 1**	Hi-Z	**Note 1**
CKE	0	**Note 2**	**Note 3**	**Note 3**	Hi-Z
RTCX1	–	–	–	–	–
RTCX2	–	–	–	–	–
CLKX1	–	–	–	–	–
CLKX2	–	–	–	–	–
FIRCLK	–	–	–	–	–
BATTINH/ BATTINT#	–	–	–	–	–
MPOWER	0	1	1	0	1
POWERON	0	0	0	0	0
POWER	–	–	–	–	–
RSTSW#	–	–	–	–	–
RTCRST#	–	–	–	–	–
RxD	–	–	–	–	–
TxD/CLKSEL2	Hi-Z[Note 4]	1	1	1	**Note 1**
RTS#/CLKSEL1	Hi-Z[Note 4]	1	1	1	**Note 1**
CTS#	–	–	–	–	–
DCD#/GPIO15	–	–	–	–	–
DTR#/CLKSEL0	Hi-Z[Note 4]	1	1	1	**Note 1**
DSR#	–	–	–	–	–
IRDIN	–	–	–	–	–
IRDOUT#	0	0	0	0	**Note 1**
FIRDIN#/SEL	Hi-Z	Hi-Z	**Note 3**	Hi-Z	**Note 3**

Notes 1. Normal operation proceeds.

2. This differs depending on the setting of the SCLK bit in the SDRAMMODEREG register.
When SCLK bit has a value of "1": outputs clock.
When SCLK bit has a value of "0": low level is output.

3. Maintains the state of the previous Full-speed Mode.

4. Specify the input data level using a high-resistance pull up or pull down resistor.

Remark 0: low level, 1: high level, Hi-Z: high impedance

(3/4)

Pin Name	After Reset by the RTC Reset	After Reset by the Deadman's Switch or RSTSW# Signal	In the Suspend Mode	In the Hibernate Mode or Shut Down by the HAL Timer	During a Bus Hold
DDIN[Note 1]/ GPIO45	–/ Hi-Z	–/ **Note 2**	–/ **Note 2**	–/ **Note 2**	– / **Note 2**
DDOUT[Note 1]/ GPIO44	1/ 1	1/ **Note 2**	1/ **Note 2**	1/ **Note 2**	1/ **Note 2**
DRTS#[Note 1]/ GPIO46	1/ 1	1/ **Note 2**	1/ **Note 2**	1/ **Note 2**	1/ **Note 2**
DCTS#[Note 1]/ GPIO47	–/ Hi-Z	–/ **Note 2**	– / **Note 2**	– / **Note 2**	–/ **Note 2**
KPORT (0:7)	–	–	–	–	–
KSCAN (0:11)[Note 1]/ GPIO (32:43)	Hi-Z/ Hi-Z	Hi-Z/ **Note 2**	**Note 2**/ **Note 2**	Hi-Z/ **Note 2**	**Note 3**
AUDIOOUT	0	0	**Note 2**	0	**Note 3**
TPX (0:1)	1	1	**Note 2**	1	**Note 3**
TPY (0:1)	Hi-Z	Hi-Z	**Note 2**	Hi-Z	**Note 3**
ADIN (0:2)	–	–	–	–	–
AUDIOIN	–	–	–	–	–
GPIO (0:3)	Hi-Z	Hi-Z	**Note 2**	Hi-Z[Note 4]	**Note 3**
SRAS#/ GPIO4	Hi-Z	**Note 5**/ Hi-Z	0/ **Note 2**	0/ Hi-Z	Hi-Z/ **Note 3**
SCAS#/ GPIO5	Hi-Z	**Note 5**/ Hi-Z	0/ **Note 2**	0/ Hi-Z	Hi-Z/ **Note 3**
SYSDIR/ GPIO6	0/ Hi-Z	0/ Hi-Z	0/ **Note 2**	0/ Hi-Z	Hi-Z/ **Note 3**
SPOWER/ GPIO7	0/ Hi-Z	1/ Hi-Z	1/ **Note 2**	1/ Hi-Z	1/ **Note 3**
GPIO (8:14)	Hi-Z	Hi-Z	**Note 2**	Hi-Z[Note 4]	**Note 3**

Notes 1. Software can switch the function pin and the output port.

2. The state of the previous Full-speed Mode is maintained.

3. Normal operation proceeds.

4. During hibernate mode, the pull-up/pull-down setting is retained.

5. When reset by RSTSW# signal: low level output (self refresh)
When reset by deadman's switch: high level output

Remark 0: low level, 1: high level, Hi-Z: high impedance

(4/4)

Pin Name	After Reset by the RTC Reset	After Reset by the Deadman's Switch or RSTSW# Signal	In the Suspend Mode	In the Hibernate Mode or Shut Down by the HAL Timer	During a Bus Hold
IRING	–	–	–	–	–
ILCSENSE	–	–	–	–	–
OFFHOOK[Note 1]	Hi-Z	Hi-Z	**Note 2**	Hi-Z	**Note 2**
MUTE[Note 1]	Hi-Z	Hi-Z	**Note 2**	Hi-Z	**Note 2**
AFERST#[Note 1]	0	0	**Note 2**	0	**Note 2**
SDI	–	–	–	–	–
FS	–	–	–	–	–
SDO	0	0	**Note 2**	0	**Note 2**
HSPSCLK	–	–	–	–	–
TELCON[Note 1]	Hi-Z	Hi-Z	**Note 2**	Hi-Z	**Note 2**
HC0[Note 1]	0	0	**Note 2**	0	**Note 2**
HSPMCLK[Note 1]	0	0	**Note 2**	0	**Note 2**
OPD#	0	0	**Note 2**	0	**Note 2**
LEDOUT#	1	**Note 3**	**Note 3**	**Note 3**	**Note 3**
DBUS32/ GPIO48[Note 4]	Hi-Z/ Hi-Z	Hi-Z/ **Note 2**	**Note 2**/ **Note 2**	Hi-Z/ **Note 2**	**Note 2**/ **Note 2**
MIPS16EN	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
SMODE1/ GPIO49[Note 4]	Hi-Z/ Hi-Z[Note 5]	Hi-Z/ **Note 2**	**Note 2**/ **Note 2**	Hi-Z/ **Note 2**	**Note 2**/ **Note 2**
SMODE2	–	–	–	–	–

Notes 1. When initializing, always set BSC bit to 1 in the HSPINT register (0x0C00 0020).

2. The state of the previous Full-speed Mode is maintained.

3. Normal operation proceeds.

4. After the RTC reset is released, this functions as an output port.

5. Specify the input data level using a high-resistance pull up or pull down resistor.

Remark 0: low level, 1: high level, Hi-Z: high impedance

1.3 Recommended Connection and I/O Circuit Types

(1/3)

Pin Name	Internal Processing	External Processing	Drive Capability	I/O Circuit Type	Recommended Connection of Unused Pins
ADD25/SCLK	Slew rate buffer	–	120 pF	A	–
ADD (0:24)	Slew rate buffer	–	120 pF	A	–
DATA (0:15)	–	–	40 pF	A	–
DATA (16:31)/ GPIO (16:31)	–	**Note 1**	40 pF	A	Connect to V_{DD} or GND via resistor
LCDCS#	Slew rate buffer	–	40 pF	A	Leave open
RD#	Slew rate buffer	**Note 2**	120 pF	A	Leave open
WR#	Slew rate buffer	**Note 2**	120 pF	A	Leave open
LCDRDY	–	**Note 3**	–	A	Connect to GND
ROMCS (2:3)#	Slew rate buffer	**Note 4**	40 pF	A	Leave open
ROMCS (0:1)#	Slew rate buffer	–	40 pF	A	Leave open
UUCAS#/MRAS3#	Slew rate buffer	**Note 2**	120 pF	A	Leave open
ULCAS#/MRAS2#	Slew rate buffer	**Note 2**	120 pF	A	Leave open
MRAS (0:1)#	Slew rate buffer	**Note 2**	40 pF	A	Leave open
UCAS#	Slew rate buffer	**Note 2**	120 pF	A	Leave open
LCAS#	Slew rate buffer	**Note 2**	120 pF	A	Leave open
BUSCLK	Slew rate buffer	–	40 pF	A	Leave open
SHB#	Slew rate buffer	**Note 2**	40 pF	A	Leave open
IOR#	Slew rate buffer	**Note 2**	40 pF	A	Leave open
IOW#	Slew rate buffer	**Note 2**	40 pF	A	Leave open
MEMR#	Slew rate buffer	**Note 2**	40 pF	A	Leave open
MEMW#	Slew rate buffer	**Note 2**	40 pF	A	Leave open
ZWS#	**Note 5**	**Note 3**	–	A	Connect to V_{DD}
RSTOUT	Slew rate buffer	Pull up	40 pF	A	Leave open
IOCS16#	**Note 5**	**Note 3**	–	A	Connect to V_{DD}
MEMCS16#	**Note 5**	**Note 3**	–	A	Connect to V_{DD}
IOCHRDY	**Note 5**	**Note 3**	–	A	Connect to GND

Notes 1. Pins DATA (16:31)/GPIO (16:31) in the VR4121 function as GPIO (16:31) signals when using the 16-bit data bus. When using these pins as GPIO (16:31) signals, pull them up or pull down so as not to input an intermediate-level signal.

2. When the bus hold function is used, external pull-up is recommended for the VR4121.

3. Do not input an intermediate-level signal.

4. When used as the RAS signal of extended DRAM, external pull-up is recommended for the VR4121.

5. When the MPOWER pin outputs the low-level, intermediate-level input is enabled.

Remarks 1. No specification (–) in the External Processing column indicates that the external processing is unnecessary.

2. No specification (–) in the Recommended Connection of Unused Pins column indicates that the pin is always connected.

(2/3)

Pin Name	Internal Processing	External Processing	Drive Capability	I/O Circuit Type	Recommended Connection of Unused Pins
HLDRQ#	**Note**	Pull up	–	A	Directly connect to V_{DD}
HLDACK#	Slew rate buffer	–	40 pF	A	Leave open
CKE	–	–	120 pF	A	Leave open
RTCX1	–	Resonator	–	–	–
RTCX2	–	Resonator	–	–	Leave open
CLKX1	–	Resonator	–	–	–
CLKX2	–	Resonator	–	–	Leave open
FIRCLK	–	Resonator	–	A	Directly connect to V_{DD}
BATTINH/ BATTINT#	Schmitt input	–	–	B	Directly connect to V_{DD}
MPOWER	–	–	40 pF	A	Leave open
POWERON	–	–	40 pF	A	Leave open
POWER	Schmitt input	–	–	B	–
RSTSW#	Schmitt input	–	–	B	–
RTCRST#	Schmitt input	–	–	B	–
RxD	–	–	–	A	Connect to GND
TxD/CLKSEL2	–	Pull up/ Pull down	40 pF	A	–
RTS#/CLKSEL1	–	Pull up/ Pull down	40 pF	A	–
CTS#	–	–	–	A	Connect to V_{DD}
DCD#/GPIO15	Schmitt input	Pull up	–	B	Connect to V_{DD} or GND
DTR#/CLKSEL0	–	Pull up/ Pull down	40 pF	A	–
DSR#	–	–	–	A	Connect to V_{DD}
IRDIN	–	Pull up	–	A	Connect to V_{DD} or GND
IRDOUT#	–	–	40 pF	A	Leave open
FIRDIN#/SEL	–	Pull up/ Pull down	40 pF	A	Connect to V_{DD} via resistor
DDIN/GPIO45	–	–	40 pF	A	Connect to V_{DD} or GND via resistor
DDOUT/GPIO44	–	–	40 pF	A	Leave open
DRTS#/GPIO46	–	–	40 pF	A	Leave open
DCTS#/GPIO47	–	–	40 pF	A	Connect to V_{DD} or GND via resistor

Note Intermediate-level input is enabled when the MPOWER pin is set for low-level output.

Remarks 1. No specification (–) in the External Processing column indicates that the external processing is unnecessary.

2. No specification (–) in the Recommended Connection of Unused Pins column indicates that the pin is always connected.

(3/3)

Pin Name	Internal Processing	External Processing	Drive Capability	I/O Circuit Type	Recommended Connection of Unused Pin
KPORT (0:7)	Schmitt input, Pull down	–	–	B	Leave open
KSCAN (0:11)/ GPIO (32:43)	–	–	40 pF	A	Leave open
AUDIOOUT	–	**Note 1**	–	F	Leave open
TPX (0:1)	–	–	120 pF or more	C	Leave open
TPY1	–	–	120 pF or more	D	Leave open
TPY0	–	–	120 pF or more	C	Leave open
ADIN (0:2)	–	–	–	E	Leave open
AUDIOIN	–	–	–	E	Leave open
GPIO (0:3)	Schmitt input, **Note 2**	**Note 2**	40 pF	B	Connect to V_{DD} or GND via resistor
SRAS#/GPIO4	Schmitt input, **Note 2**	**Note 2**	40 pF	B	Connect to V_{DD} or GND
SCAS#/GPIO5	Schmitt input, **Note 2**	**Note 2**	40 pF	B	Connect to V_{DD} or GND
SYSDIR/GPIO6	Schmitt input, **Note 2**	**Note 2**	40 pF	B	Leave open
SPOWER/GPIO7	Schmitt input, **Note 2**	**Note 2**	40 pF	B	Connect to V_{DD} or GND
GPIO (8:14)	Schmitt input, **Note 2**	**Note 2**	40 pF	B	Connect to V_{DD} or GND via resistor
IRING	Schmitt input	Pull down	–	B	Connect to GND
ILCSENSE	–	Pull down	–	A	Connect to GND
OFFHOOK	–	–	40 pF	A	Leave open
MUTE	–	–	40 pF	A	Leave open
AFERST#	–	–	40 pF	A	Leave open
SDI	–	Pull up/Pull down	–	A	Connect to GND
FS	–	Pull up/Pull down	–	A	Connect to GND
SDO	–	–	40 pF	A	Leave open
HSPSCLK	–	**Note 3**	–	A	Connect to GND
TELCON	–	–	40 pF	A	Leave open
HC0	–	–	40 pF	A	Leave open
HSPMCLK	–	–	40 pF	A	Leave open
OPD#	–	–	40 pF	A	Leave open
LEDOUT#	–	–	40 pF	A	Leave open
DBUS32/GPIO48	–	Pull up/Pull down	40 pF	A	–
MIPS16EN	–	Pull up/Pull down	40 pF	A	–
SMODE1/GPIO49	–	Pull up/Pull down	–	A	–
SMODE2	–	Pull up/Pull down	–	A	–

Notes 1. Connect an operation amplifier which has high-impedance input characteristics, since the output level of AUDIOOUT pin varies according to the external impedance.

2. If internal pull-up or pull-down resistors are used in GPIO (0:3), SRAS#/GPIO4, SCAS#/GPIO5, SYSDIR/GPIO6, SPOWER/GPIO7, GPIO (8:14) pins switch between pull up, pull down, and open by software.

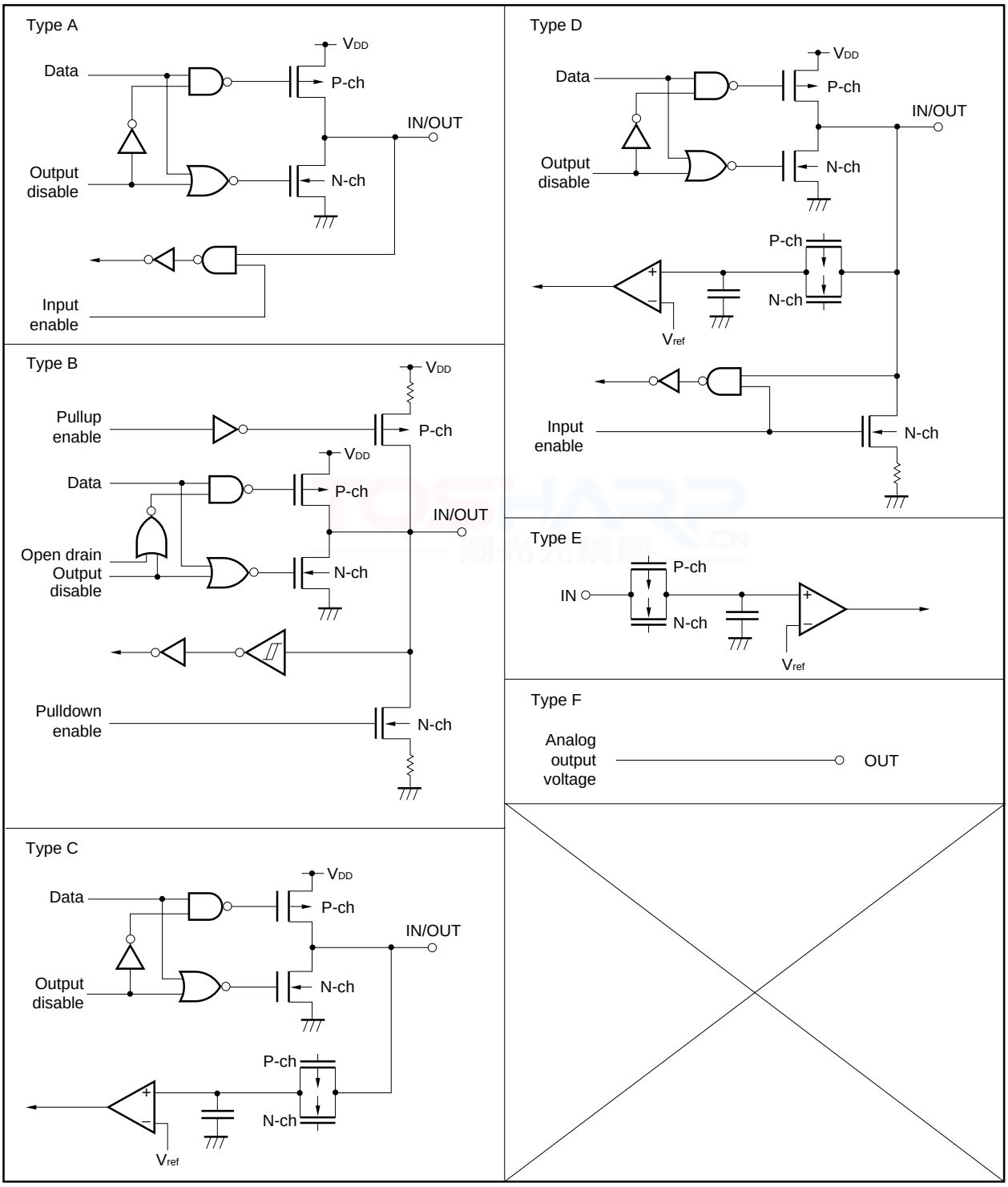
If an internal pull-up or pull-down resistor is not used, then provide an external pull-up or pull-down resistor.

3. Input a synchronous clock from CODEC.

Remarks 1. No specification (–) in the External Processing column indicates that the external processing is unnecessary.

2. No specification (–) in the Recommended Connection of Unused Pins column indicates that the pin is always connected.

1.4 Pin I/O Circuits



2. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD2}	2.5 V (V_{DD}P, V_{DD}PD, V_{DD}2)	–0.5 to +3.3	V
	V_{DD3}	3.3 V (CV_{DD}, DV_{DD}, AV_{DD}, $PIUV_{DD}$, V_{DD}3)	–0.5 to +4.0	V
Input voltage	V_I	$V_{DD3} \geq 3.7$ V	–0.5 to +4.0	V
		$V_{DD3} < 3.7$ V	–0.5 to V_{DD3} + 0.3	V
Storage temperature	T_{stg}		–65 to +150	°C

Cautions 1. Do not short-circuit two or more output pins simultaneously.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The specifications and conditions shown in DC Characteristics and AC Characteristics are the ranges for normal operation and quality assurance of the product.

3. V_I can be –1.5 V if the input pulse is less than 10 ns.

Operating Conditions

(1) 131 MHz model

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Supply voltage	V_{DD2}	2.5 V (V_{DD}P, V_{DD}PD, V_{DD}2)	2.3	2.7	V
	V_{DD3}	3.3 V (CV_{DD}, DV_{DD}, AV_{DD}, $PIUV_{DD}$, V_{DD}3)	3.0	3.45	V
Ambient temperature	T_A		–10	+70	°C
Oscillation start voltage[Note 1]	V_{DDS}			3.0	V
Oscillation hold voltage[Note 2]	V_{DDH1}			2.5	V
Oscillation hold voltage[Note 3]	V_{DDH2}			3.0	V

Notes 1. This is a voltage at which oscillation is always started after power application, and is applied to oscillators of 32.768 kHz and 18.432 MHz.

2. This is a voltage at which oscillation can be guaranteed if the voltage is lowered from the normal operation level, and is applied to an oscillator of 32.768 kHz.

3. This is a voltage at which oscillation can be guaranteed if the voltage is lowered from the normal operation level, and is applied to an oscillator of 18.432 MHz.

(2) 168 MHz model

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Supply voltage	V_{DD2}	2.5 V (V_{DD}P, V_{DD}PD, V_{DD}2)	2.6	2.7[Note 1]	V
	V_{DD3}	3.3 V (CV_{DD}, DV_{DD}, AV_{DD}, $PIUV_{DD}$, V_{DD}3)	3.0	3.45	V
Ambient temperature	T_A		–10	+70	°C
Oscillation start voltage[Note 2]	V_{DDS}			3.0	V
Oscillation start voltage[Note 3]	V_{DDH1}			2.5	V
Oscillation start voltage[Note 4]	V_{DDH2}			3.0	V

Notes 1. If V_{DD2} exceeds 2.7 V, be sure to keep the time for which the voltage is exceeded to less than 10 % of the total operating time of the V_R4121, and the maximum value of V_{DD2} to less than 2.8 V.

2. This is a voltage at which oscillation is always started after power application, and is applied to oscillators of 32.768 kHz and 18.432 MHz.

3. This is a voltage at which oscillation can be guaranteed if the voltage is lowered from the normal operation level, and is applied to an oscillator of 32.768 kHz.

4. This is a voltage at which oscillation can be guaranteed if the voltage is lowered from the normal operation level, and is applied to an oscillator of 18.432 MHz.

Capacitance (T_A = 25°C, V_{DD} = 0 V)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz		10	pF
I/O capacitance	C_{IO}	Unmeasured pins returned to 0 V.		10	pF

Caution Precision tests have not been performed. Only guaranteed as design characteristics.

DC Characteristics

(1) 131 MHz model (T_A = –10 to +70°C, V_{DD2} = 2.3 to 2.7 V, V_{DD3} = 3.0 to 3.45 V)

(1/2)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	I_{OH} = –2 mA	0.8V_{DD3}			V
Output voltage, high[Note 1]	V_{OH2}	I_{OH} = –12 mA	0.8V_{DD3}			V
Output voltage, low	V_{OL1}	I_{OL} = 2 mA			0.4	V
		I_{OL} = 20 μA			0.1	
Output voltage, low[Note 1]	V_{OL2}	I_{OL} = 12 mA			0.4	V
		I_{OL} = 20 μA			0.1	
Clock input voltage, high[Note 2]	V_{IH1}		0.8 V_{DD3}		V_{DD3} + 0.3	V
Clock input voltage, low[Note 2]	V_{IL1}		–0.3		0.3 V_{DD3}	V
Input voltage, high[Note 3]	V_{IH2}		2.0		V_{DD3} + 0.3	V
Input voltage, low[Note 3]	V_{IL2}		–0.3		0.3V_{DD3}	V
Input voltage, high[Note 4]	V_{IH3}		0.75V_{DD3}		V_{DD3} + 0.3	V
Input voltage, low[Note 4]	V_{IL3}		–0.3		0.6	V
Hysteresis voltage[Note 4, 5]	V_H			0.17V_{DD3}		V
Input leakage current[Note 6]	I_{LI}	V_{DD3} = 3.45 V, V_I = V_{DD3}, 0 V			±5	μA
Input leakage current, high[Note 7]	I_{LIH}	V_{DD3} = 3.45 V, V_I = V_{DD3}			72	μA
Input leakage current, low[Note 8]	I_{LIL}	V_{DD3} = 3.45 V, V_I = 0 V			–72	μA
Output leakage current	I_{LO}	V_{DD3} = 3.45 V, V_I = V_{DD3}, 0 V			±5	μA

Notes 1. Applied to TPX (0:1), TPY (0:1). A panel resistance of 250 Ω is presumed.

2. Applies to FIRCLK and HSPSCLK pins.

3. Except RTCX1, CLKX1, FIRCLK, HSPSCLK, TPX (0:1), TPY (0:1), ADIN (0:2), AUDIOIN, POWER, RSTSW#, RTCRST#, GPIO (0:3), SRAS#/GPIO4, SCAS#/GPIO5, SYDIR/GPIO6, SPOWER/GPIO7, GPIO (8:14), DCD#/GPIO15, BATTINH/BATTINT#, IRING, and KPORT (0:7) pins.

4. Applied to POWER, RSTSW#, RTCRST#, GPIO (0:3), SRAS#/GPIO4, SCAS#/GPIO5, SYDIR/GPIO6, SPOWER/GPIO7, GPIO (8:14), DCD#/GPIO15, BATTINH/BATTINT#, IRING, and KPORT (0:7) pins.

5. Hysteresis voltage: Difference between the minimum voltage at which the high level of a Schmitt input signal is not recognized when the signal goes from low to high and the maximum voltage at which the low level is not recognized when the signal goes from high to low.

6. Except KPORT (0:7) (input pins with pull-down resistor), TPX (0:1), and TPY (0:1) pins.

7. Applied to KPORT (0:7) pin (input pins with pull-down resistor), GPIO (0:3), SRAS#/GPIO4, SCAS#/GPIO5, SYSDIR/GPIO6, SPOWER/GPIO7, and GPIO (8:14) pins when the internal pull-down resistor is used.

8. Applied to GPIO (0:3), SRAS#/GPIO4, SCAS#/GPIO5, SYSDIR/GPIO6, SPOWER/GPIO7, and GPIO (8:14) pins when the internal pull-up resistor is used.

(2/2)

Parameter	Symbol	Condition	MIN.	TYP. Note 1	MAX.	Unit
Power supply current	I_{DD2} Note 2	In Fullspeed mode		140	340	mA
		In Standby mode		50	100	mA
		In Suspend mode		15	30	mA
		In Hibernate mode, V_{DD2} = 0.0 V, when LED unit is off.		0	0	μA
	I_{DD3} Note 3	In Fullspeed mode, ADD (0:24), ADD25/SCLK, CKE, RD#, WR#, TPX (0:1), TPY (0:1) = 120 pF, other pins = 40 pF		30	60	mA
		In Standby mode, external load 0 pF		10	30	mA
		In Suspend mode, external load 0 pF		3	9	mA
		In Hibernate mode, external load 0 pF, when LED unit is off.		100	500	μA

Notes 1. Unless otherwise specified, these are reference values at T_A = 25°C, V_{DD2} = 2.5 V, V_{DD3} = 3.3 V.

2. Total current flowing to the V_{DD}P, V_{DD}PD, and V_{DD}2 pins.

3. Total current flowing to the CV_{DD}, DV_{DD}, AV_{DD}, $PIUV_{DD}$, and V_{DD}3 pins.

Remark I_{DD2} and I_{DD3} do not reach the maximum value at the same time in the Fullspeed mode.

(2) 168 MHz model (T_A = –10 to +70°C, V_{DD2} = 2.6 to 2.7 V, V_{DD3} = 3.0 to 3.45 V)

(1/2)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	I_{OH} = –2 mA	0.8V_{DD3}			V
Output voltage, high[Note 1]	V_{OH2}	I_{OH} = –12 mA	0.8V_{DD3}			V
Output voltage, low	V_{OL1}	I_{OL} = 2 mA			0.4	V
		I_{OL} = 20 μA			0.1	
Output voltage, low[Note 1]	V_{OL2}	I_{OL} = 12 mA			0.4	V
		I_{OL} = 20 μA			0.1	
Clock input voltage, high[Note 2]	V_{IH1}		0.8 V_{DD3}		V_{DD3} + 0.3	V
Clock input voltage, low[Note 2]	V_{IL1}		–0.3		0.3 V_{DD3}	V
Input voltage, high[Note 3]	V_{IH2}		2.0		V_{DD3} + 0.3	V
Input voltage, low[Note 3]	V_{IL2}		–0.3		0.3V_{DD3}	V
Input voltage, high[Note 4]	V_{IH3}		0.75V_{DD3}		V_{DD3} + 0.3	V
Input voltage, low[Note 4]	V_{IL3}		–0.3		0.6	V
Hysteresis voltage[Note 4, 5]	V_H			0.17V_{DD3}		V
Input leakage current[Note 6]	I_{LI}	V_{DD3} = 3.45 V, V_I = V_{DD3}, 0 V			±5	μA
Input leakage current, high[Note 7]	I_{LIH}	V_{DD3} = 3.45 V, V_I = V_{DD3}			72	μA
Input leakage current, low[Note 8]	I_{LIL}	V_{DD3} = 3.45 V, V_I = 0 V			–72	μA
Output leakage current	I_{LO}	V_{DD3} = 3.45 V, V_I = V_{DD3}, 0 V			±5	μA

Notes 1. Applied to TPX (0:1), TPY (0:1). A panel resistance of 250 Ω is presumed.

2. Applies to FIRCLK and HSPSCLK pins.

3. Except RTCX1, CLKX1, FIRCLK, HSPSCLK, TPX (0:1), TPY (0:1), ADIN (0:2), AUDIOIN, POWER, RSTSW#, RTCRST#, GPIO (0:3), SRAS#/GPIO4, SCAS#/GPIO5, SYDIR/GPIO6, SPOWER/GPIO7, GPIO (8:14), DCD#/GPIO15, BATTINH/BATTINT#, IRING, and KPORT (0:7) pins.

4. Applied to POWER, RSTSW#, RTCRST#, GPIO (0:3), SRAS#/GPIO4, SCAS#/GPIO5, SYDIR/GPIO6, SPOWER/GPIO7, GPIO (8:14), DCD#/GPIO15, BATTINH/BATTINT#, IRING, and KPORT (0:7) pins.

5. Hysteresis voltage: Difference between the minimum voltage at which the high level of a Schmitt input signal is not recognized when the signal goes from low to high and the maximum voltage at which the low level is not recognized when the signal goes from high to low.

6. Except KPORT (0:7) (input pins with pull-down resistor), TPX (0:1), and TPY (0:1) pins.

7. Applied to KPORT (0:7) pin (input pins with pull-down resistor), GPIO (0:3), SRAS#/GPIO4, SCAS#/GPIO5, SYSDIR/GPIO6, SPOWER/GPIO7, and GPIO (8:14) pins when the internal pull-down resistor is used.

8. Applied to GPIO (0:3), SRAS#/GPIO4, SCAS#/GPIO5, SYSDIR/GPIO6, SPOWER/GPIO7, and GPIO (8:14) pins when the internal pull-up resistor is used.

(2/2)

Parameter	Symbol	Condition	MIN.	TYP. Note 1	MAX.	Unit
Power supply current	I_{DD2} Note 2	In Fullspeed mode		180	370	mA
		In Standby mode		50	100	mA
		In Suspend mode		15	30	mA
		In Hibernate mode, V_{DD2} = 0.0 V, when LED unit is off.		0	0	μA
	I_{DD3} Note 3	In Fullspeed mode, ADD (0:24), ADD25/SCLK, CKE, RD#, WR#, TPX (0:1), TPY (0:1) = 120 pF, other pins = 40 pF		30	60	mA
		In Standby mode, external load 0 pF		10	30	mA
		In Suspend mode, external load 0 pF		3	9	mA
		In Hibernate mode, external load 0 pF, when LED unit is off.		100	500	μA

Notes 1. Unless otherwise specified, these are reference values at T_A = 25°C, V_{DD2} = 2.6 V, V_{DD3} = 3.3 V.

2. Total current flowing to the V_{DD}P, V_{DD}PD, and V_{DD}2 pins.

3. Total current flowing to the CV_{DD}, DV_{DD}, AV_{DD}, $PIUV_{DD}$, and V_{DD}3 pins.

Remark I_{DD2} and I_{DD3} do not reach the maximum value at the same time in the Fullspeed mode.

Data Retention Characteristics (T_A = 25°C)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data retention voltage[Note 1]	V_{DDDR3}	Hibernate mode, 3.3 V power supply	2.5	3.45	V
Data retention input voltage, high[Note 2]	V_{IHDR}		$0.9V_{DDDR3}$		V

Notes 1. The data retention voltage is the voltage at which the operation of the Elapsed Time timer and the data retention of the registers of the following peripheral units are guaranteed, and is not applied to the internal data of the CPU core.

BCU: BCURFCNTREG, BCUCNTREG3, SDRAMMODEREG, SROMMODEREG, SDRAMCNTREG
PUM: PMUCNTREG (15:8), PMUCNT2REG, PMUWAITREG, PMUDIVREG
RTC: ETIMELREG, ETIMEMREG, ETIMEHREG, ECMPLREG, ECMPMREG, ECMPHREG, RTCL1LREG, RTCL1HREG, RTCL1CNTLREG, RTCL1CNTHREG, RTCL2LREG, RTCL2HREG, RTCL2CNTLREG, RTCL2CNTHREG, RTCINTREG (2:0)
GIU: GIUPODATL, GIUPODATH, GIUUSEUPNL, GIUTERMUPNL
KIU: KIUGPEN, PORTREG
LED: LEDHTSREG, LEDLTSREG, LEDHLTCLREG, LEDHLTCHREG, LEDCNTREG

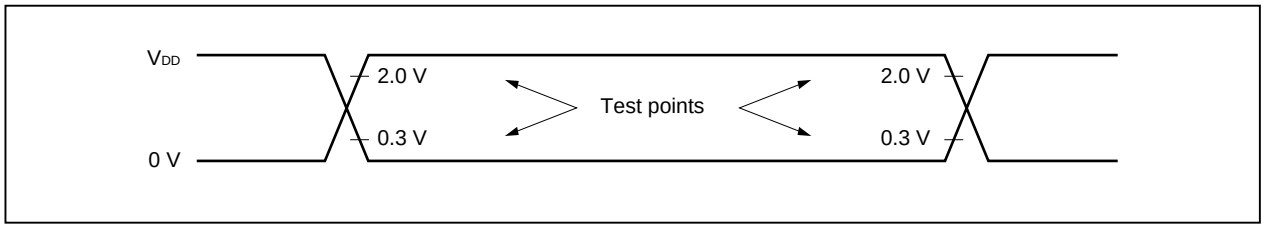
2. Applied to RTCRST# pin.

Remark The values in parentheses are the targeted values.

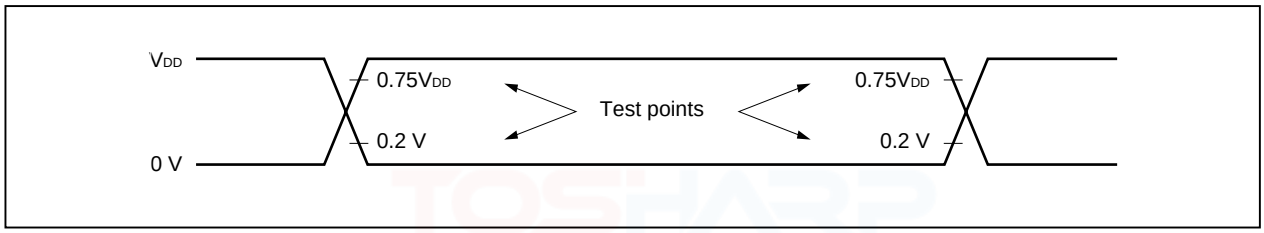
AC Characteristics (131 MHz model: T_A = –10 to +70°C, V_{DD2} = 2.3 to 2.7 V, V_{DD3} = 3.0 to 3.45 V
168 MHz model: T_A = –10 to +70°C, V_{DD2} = 2.6 to 2.7 V, V_{DD3} = 3.0 to 3.45 V)

AC test input waveform

(a) CTS#, DATA (0:15), DATA (16:31)/GPIO (16:31), DBUS32/GPIO48, DCTS#/GPIO47, DDIN/GPIO45, DSR#, DTR#/CLKSEL0, FS, FIRDIN#/SEL, HLDRQ#, ILCSENSE, IOCHRDY, IOCS16#, IRDIN, LCDRDY, MEMCS16#, RxD, RTS#/CLKSEL1, SDI, SMODE1/GPIO49, SMODE2, TxD/CLKSEL2, ZWS#

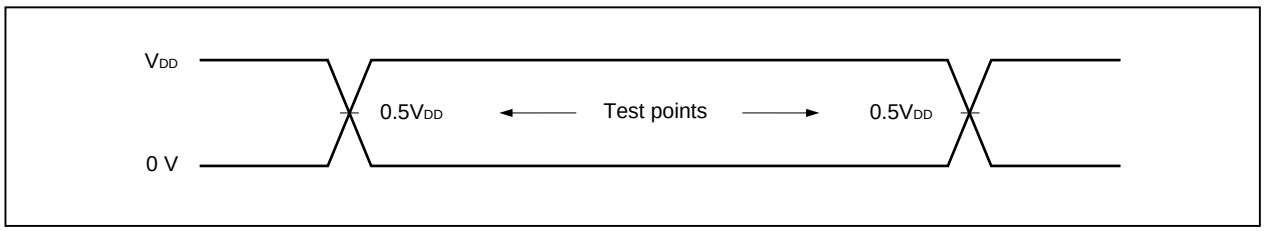


(b) BATTINH/BATTINT#, DCD#/GPIO15, GPIO (0:3), GPIO (8:14), IRING, KPORT (0:7), POWER, RSTSW#, RTCRST#, SCAS#/GPIO5, SPOWER/GPIO7, SRAS#/GPIO4, SYSDIR/GPIO6



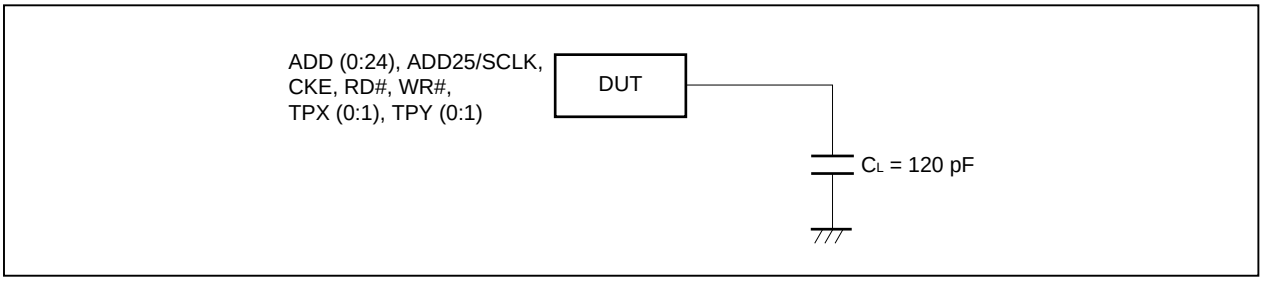
AC test output measuring points

(c) ADD (0:24), ADD25/SCLK, AFERST#, BUSCLK, CKE, DATA (0:15), DATA (16:31)/GPIO (16:31), DBUS32/GPIO48, DCTS#/GPIO47, DDIN/GPIO45, DDOUT/GPIO44, DRTS#/GPIO46, DTR#/CLKSEL0, FIRDIN#/SEL, GPIO (0:3), GPIO (8:14), HC0, HLDACK#, HSPMCLK, IOR#, IOW#, IRDOUT#, KSCAN (0:11)/GPIO (32:43), LCAS#, LCDCS#, LEDOUT#, MEMR#, MEMW#, MPOWER, MRAS (0:1)#, MUTE, OFFHOOK, OPD#, POWERON, RD#, ROMCS (0:3)#, RSTOUT, RTS#/CLKSEL1, SCAS#/GPIO5, SDO, SHB#, SMODE1/GPIO49, SPOWER/GPIO7, SRAS#/GPIO4, SYSDIR/GPIO6, TELCON, TPX (0:1), TPY (0:1), TxD/CLKSEL2, UCAS#, ULCAS#/MRAS2#, UUCAS#/MRAS3#, WR#

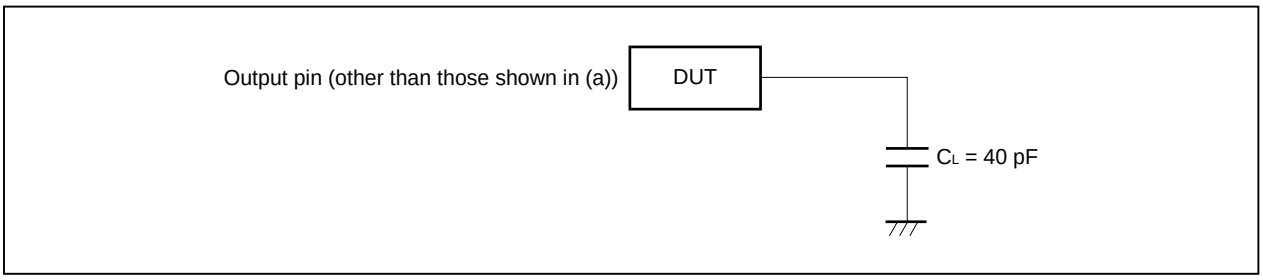


Load condition

(a) ADD (0:24), ADD25/SCLK, CKE, RD#, WR#, TPX (0:1), TPY (0:1)



(b) Other output pins



(1) Clock parameter (1/2)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
HSPSCLK high-level width	t_{WHSH}	When HSP unit is used	40			ns
HSPSCLK low-level width	t_{WHSL}	When HSP unit is used	40			ns
HSPSCLK clock frequency	f_{HSCYC}	When HSP unit is used			f_{MCYC}	MHz
HSPSCLK clock cycle	t_{CYHS}	When HSP unit is used	108.5			ns
HSPSCLK clock rise time	t_{HSR}	When HSP unit is used			10	ns
HSPSCLK clock fall time	t_{SHF}	When HSP unit is used			10	ns
HSPMCLK high-level width	t_{MPH}	When HSP unit is used	$t_{CYHM} \times 0.45$		$t_{CYHM} \times 0.55$	ns
HSPMCLK low-level width	t_{MPL}	When HSP unit is used	$t_{CYHM} \times 0.45$		$t_{CYHM} \times 0.55$	ns
HSPMCLK clock frequency	f_{MCYC}	When HSP unit is used	0.585		18.432	MHz
HSPMCLK clock cycle	t_{CYHM}	When HSP unit is used	54.253		1790.365	ns
FIRCLK clock frequency	$f_{FIRCYC1}$	In FIR 4 Mbps	47.99520	48	48.00480	MHz
	$f_{FIRCYC2}$	In FIR 1.152/0.576 Mbps	47.93800	48	48.02976	MHz
FIRCLK clock duty	$t_{FIRDUTY}$		10		90	%
SCLK high-level width[Note 1]	t_{CH}		3.5			ns
SCLK low-level width[Note 1]	t_{CL}		3.5			ns
SCLK jitter[Note 2]	t_{Jitter}				3.5	%
CPU core operating frequency	f_{PCYC}	CLKSEL (2:0) = 111[Note 3]		RFU		MHz
		CLKSEL (2:0) = 110[Note 4]		168.5		MHz
		CLKSEL (2:0) = 101[Note 4]		147.5		MHz
		CLKSEL (2:0) = 100		131.1		MHz
		CLKSEL (2:0) = 011		118.0		MHz
		CLKSEL (2:0) = 010		98.3		MHz
		CLKSEL (2:0) = 001		90.7		MHz
		CLKSEL (2:0) = 000		78.6		MHz
BUSCLK high-level width	t_{BCLKH1}	**Note 5**	45			ns
	t_{BCLKH2}	**Note 6**	10			ns
BUSCLK low-level width	t_{BCLKL1}	**Note 5**	45			ns
	t_{BCLKL2}	**Note 6**	10			ns

Notes 1. Applied to ADD25/SCLK pin.

2. Precision tests have not been performed. Only guaranteed as design characteristics.

3. Do not set CLKSEL (2:0) = 111.

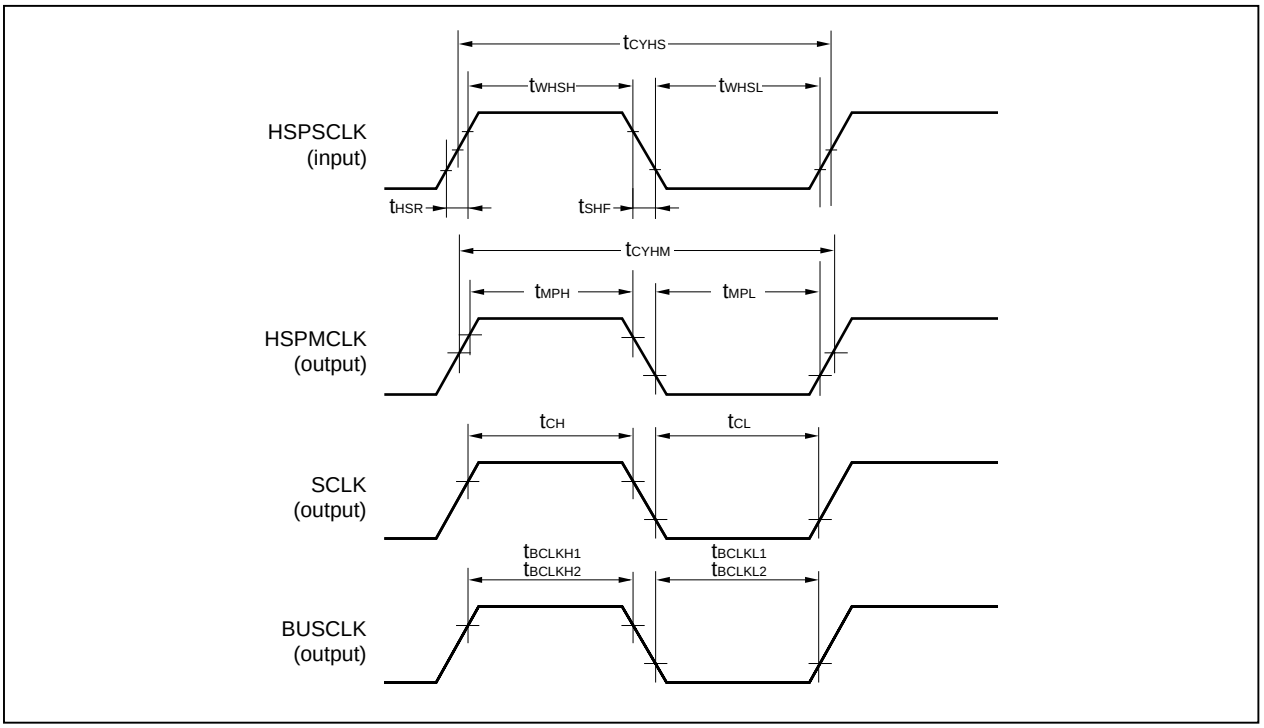
4. The settings CLKSEL (2:0) = 110 and 101 are only guaranteed for the 168 MHz model. Do not apply these settings to the 131 MHz model.

5. Applied to BUSCLK pin when BSEL bit of BCUCNTREG3 register is 0.

6. Applied to BUSCLK pin when BSEL bit of BCUCNTREG3 register is 1.

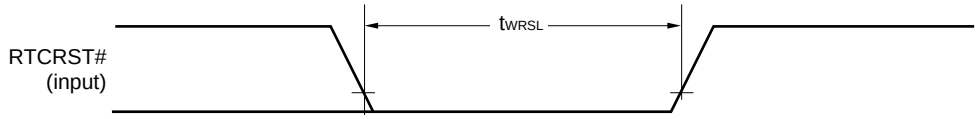
Remark CLKSEL (2:0): Value set to the TxD/CLKSEL2, RTS#/CLKSEL1, and DTR#/CLKSEL0 pins after reset.

(1) Clock parameter (2/2)



(2) Reset parameter

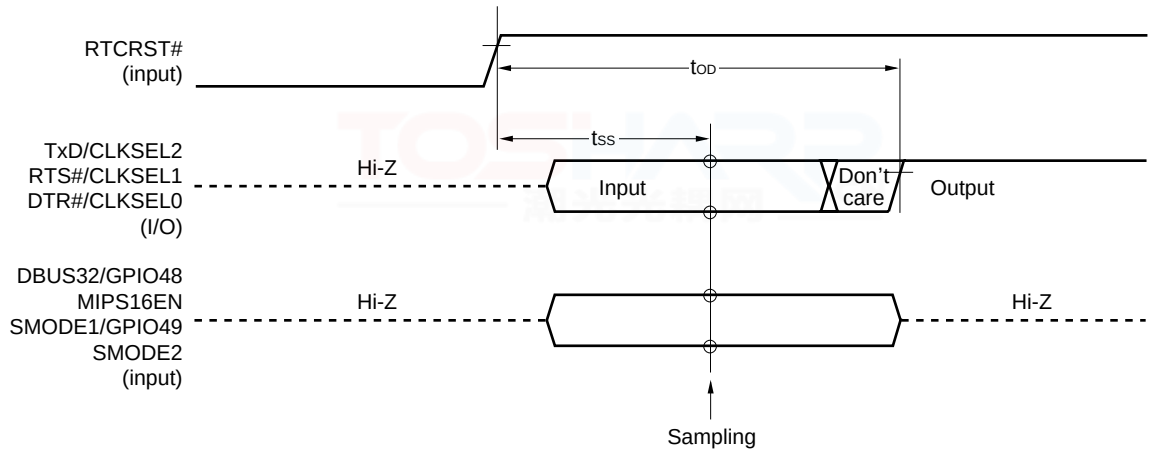
Parameter	Symbol	Condition	MIN.	MAX.	Unit
Reset input low-level width	t_{WRSL}	RTCRST#	305		μs



Remark For the RTCRST# characteristics at power application, refer to **VR4121 User's Manual**.

(3) Initialization parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data sampling time (from RTCRST# ↑)	t_{SS}			61.04	μs
Output delay time (from RTCRST# ↑)	t_{OD}		61.04		μs



Remark Set the input data level by using a pull-up or pull-down resistor with high resistance.

(4) GPIO interface parameter (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input level width	t_{INP1}	**Note 1**	91.5		μs
	t_{INP2}	**Note 2**	361.5		ns
	t_{INP3}	**Note 3**	180.6		ns
GPIO input rise time	t_{GPINR1}	**Note 4**		200	ns
	t_{GPINR2}	**Note 5**		10	ns
GPIO input fall time	t_{GPINF1}	**Note 4**		200	ns
	t_{GPINF2}	**Note 5**		10	ns
Output level width	t_{OUTP}	**Note 6**	30		ns

Notes 1. Applied to GPIO (0:3) pins.

2. Applied to GPIO (9:14) and DCD#/GPIO15 pins.

3. Applied to SRAS#/GPIO4, SCAS#/GPIO5, SYSDIR/GPIO6, SPOWER/GPIO7, GPIO8, and DATA (16:31)/GPIO (16:31) pins.

4. Applied to GPIO (0:3), SRAS#/GPIO4, SCAS#/GPIO5, SYSDIR/GPIO6, SPOWER/GPIO7, GPIO (8:14), and DCD#/GPIO15 pins.

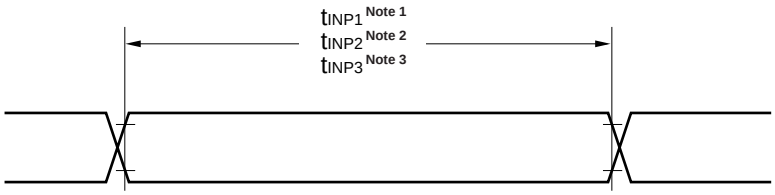
5. Applied to DATA (16:31)/GPIO (16:31) pins.

6. Applied to GPIO (0:3), SRAS#/GPIO4, SCAS#/GPIO5, SYSDIR/GPIO6, SPOWER/GPIO7, GPIO (8:14), DATA (16:31)/GPIO (16:31), KSCAN (0:11)/GPIO (32:43), DDOUT/GPIO44, DDIN/GPIO45, DRTS#/GPIO46, DCTS#/GPIO47, DBUS32/GPIO48, and SMODE1/GPIO49 pins.

Caution These parameters are applied when the SRAS#/GPIO4, SCAS#/GPIO5, SYSDIR/GPIO6, SPOWER/GPIO7, DCD#/GPIO15, DATA (16:31)/GPIO (16:31), KSCAN (0:11)/GPIO (32:43), DDOUT/GPIO44, DDIN/GPIO45, DRTS#/GPIO46, DCTS#/GPIO47, DBUS32/GPIO48, or SMODE1/GPIO49 pin is used as the GPIO signal.

(4) GPIO interface parameter (2/2)

(a) Input level width

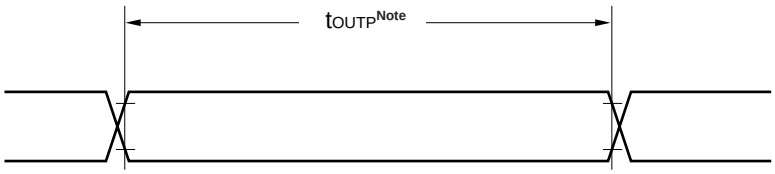


Notes 1. GPIO (0:3) pins
2. GPIO (9:14), DCD#/GPIO15 pins
3. SRAS#/GPIO4, SCAS#/GPIO5, SYSDIR/GPIO6, SPOWER/GPIO7, GPIO8, DATA (16:31)/GPIO (16:31) pins

(b) GPIO input rise/fall time

Notes 1. GPIO (0:3), SRAS#/GPIO4, SCAS#/GPIO5, SYSDIR/GPIO6, SPOWER/GPIO7, GPIO (8:14), DCD#/GPIO15 pins
2. DATA (16:31)/GPIO (16:31) pins

(c) Output level width



Note GPIO (0:3), SRAS#/GPIO4, SCAS#/GPIO5, SYSDIR/GPIO6, SPOWER/GPIO7, GPIO (8:14), DATA (16:31)/GPIO (16:31), KSCAN (0:11)/GPIO (32:43), DDOUT/GPIO44, DDIN/GPIO45, DRTS#/GPIO46, DCTS#/GPIO47, DBUS32/GPIO48, SMODE1/GPIO49 pins

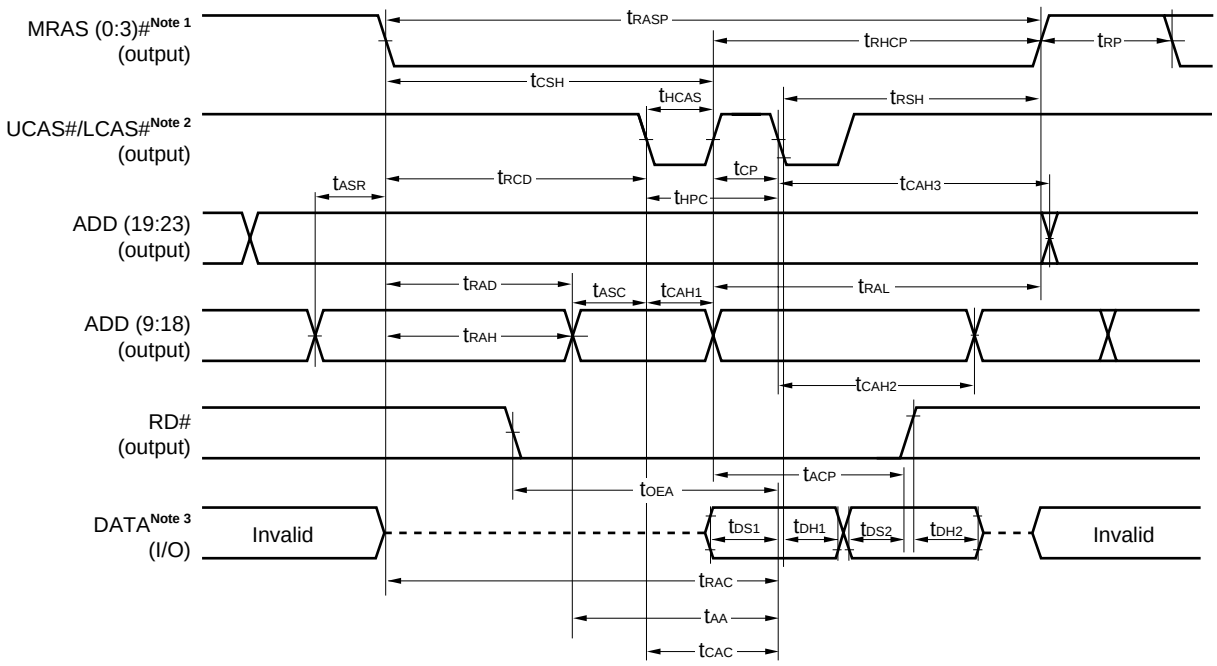
(5) EDO-type DRAM read parameter (1/2)

The target DRAM is the μPD42S16165L-A60, 42S18165L-A60, 42S64165G5-A50, 42S64165G5-A60, 42S65165G5-A50, or 42S65165G5-A60.

Parameter	Symbol	Condition	MIN.	MAX.	Unit
MRAS (0:3)# pulse width	t_{RASP}		70		ns
MRAS (0:3)# hold time (from UCAS#/LCAS# precharge)	t_{RHCP}		45		ns
MRAS (0:3)# precharge time	t_{RP}		43		ns
UCAS#/LCAS# hold time (from MRAS (0:3)#)	t_{CSH}		50		ns
UCAS#/LCAS# pulse width	t_{HCAS}		10		ns
UCAS#/LCAS# precharge time	t_{CP}		10		ns
Read/write cycle time	t_{HPC}		25		ns
MRAS (0:3)# hold time (from UCAS#/LCAS#)	t_{RSH}		25		ns
Row address setup time (to MRAS (0:3)#)	t_{ASR}		0		ns
UCAS#/LCAS# ↓ delay time from MRAS (0:3)# ↓	t_{RCD}		24		ns
Column address delay time from MRAS (0:3)# ↓	t_{RAD}		22		ns
Column address setup time (to UCAS#/LCAS#)	t_{ASC}		0		ns
Column address read time (to MRAS (0:3)#↑)	t_{RAL}		40		ns
Row address hold time (from MRAS (0:3)# ↓)	t_{RAH}		20		ns
Column address hold time 1 (from UCAS#/LCAS# ↓)	t_{CAH1}		10		ns
Column address hold time 2 (from UCAS#/LCAS# ↓)	t_{CAH2}		10		ns
Column address hold time 3 (from UCAS#/LCAS# ↓)	t_{CAH3}		10		ns
Data access time (from UCAS#/LCAS# precharge)	t_{ACP}		39		ns
Data access time (from RD# ↓)	t_{OEA}		25		ns
Data input setup time 1 (to UCAS#/LCAS# ↓)	t_{DS1}		0		ns
Data input hold time 1 (from MRAS (0:3)#)	t_{DH1}		5		ns
Data input setup time 2 (to UCAS#/LCAS# ↓)	t_{DS2}		0		ns
Data input hold time 2 (from MRAS (0:3)#)	t_{DH2}		5		ns
Data access time (from MRAS (0:3)# ↓)	t_{RAC}		70		ns
Data access time (from column address)	t_{AA}		30		ns
Data access time (from UCAS#/LCAS# ↓)	t_{CAC}		20		ns

Caution These ratings are applied only when a device operates within the recommended operating condition range and the operating ambient temperature is kept constant.
If the power supply voltage or operating ambient temperature changes during DRAM access, the above ratings are not applied.

(5) EDO-type DRAM read parameter (2/2)



Notes 1. In 32-bit mode: Applied to MRAS (0:1)# pins
In 16-bit mode: Applied to UUCAS#/MRAS3#, ULCAS#/MRAS2#, and MRAS (0:1)# pins

2. In 32-bit mode: Applied to UUCAS#/MRAS3#, ULCAS#MRAS2#, UCAS#, and LCAS# pins
In 16-bit mode: Applied to UCAS# and LCAS# pins

3. In 32-bit mode: Applied to DATA (16:31)/GPIO (16:31) and DATA (0:15) pins
In 16-bit mode: Applied to DATA (0:15) pins

Remark The broken lines indicate high impedance.

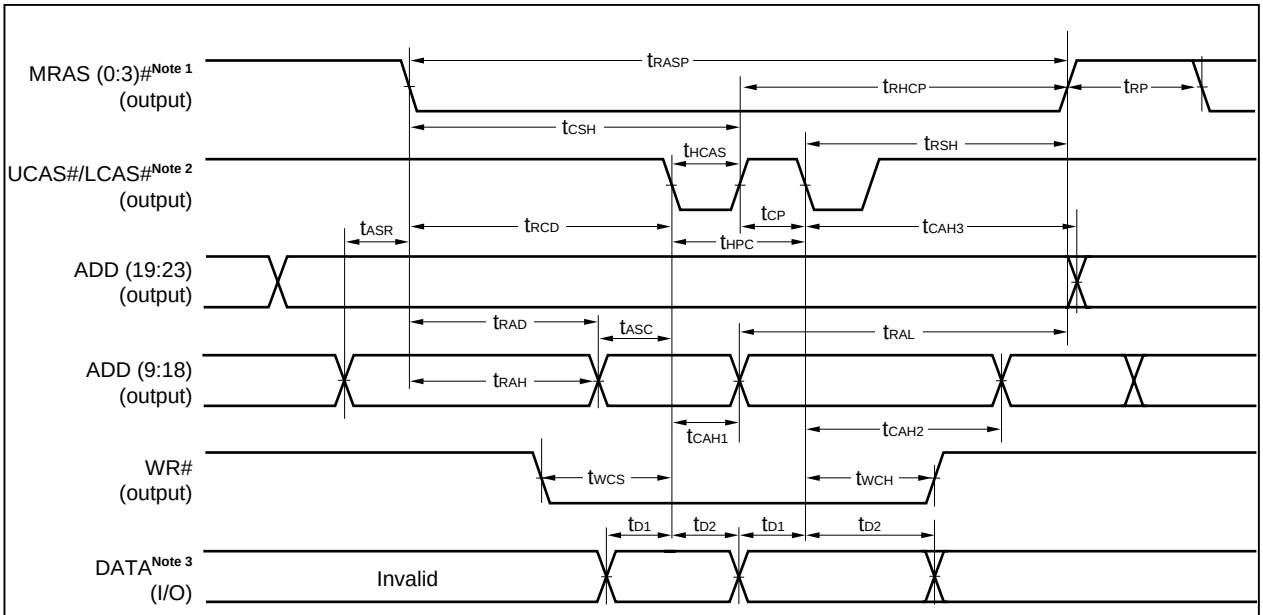
(6) EDO-type DRAM write parameter (1/2)

The target DRAM is the μPD42S16165L-A60, 42S18165L-A60, 42S64165G5-A50, 42S64165G5-A60, 42S65165G5-A50, or 42S65165G5-A60.

Parameter	Symbol	Condition	MIN.	MAX.	Unit
MRAS (0:3)# pulse width	t_{RASP}		70		ns
MRAS (0:3)# hold time (from UCAS#/LCAS# precharge)	t_{RHCP}		45		ns
MRAS (0:3)# precharge time	t_{RP}		43		ns
UCAS#/LCAS# hold time (from MRAS (0:3)# ↓)	t_{CSH}		50		ns
UCAS#/LCAS# pulse width	t_{HCAS}		10		ns
UCAS#/LCAS# precharge time	t_{CP}		10		ns
Read/write cycle time	t_{HPC}		25		ns
MRAS (0:3)# hold time (from UCAS#/LCAS#)	t_{RSH}		25		ns
Row address setup time (to MRAS (0:3)# ↓)	t_{ASR}		0		ns
UCAS#/LCAS# ↓ delay time from MRAS (0:3)# ↓	t_{RCD}		24		ns
Column address delay time from MRAS (0:3)# ↓	t_{RAD}		22		ns
Column address setup time (to UCAS#/LCAS# ↓)	t_{ASC}		0		ns
Column address read time (to MRAS (0:3)# ↑)	t_{RAL}		40		ns
Row address hold time (from MRAS (0:3)# ↓)	t_{RAH}		20		ns
Column address hold time 1 (from UCAS#/LCAS# ↓)	t_{CAH1}		10		ns
Column address hold time 2 (from UCAS#/LCAS# ↓)	t_{CAH2}		10		ns
Column address hold time 3 (from UCAS#/LCAS# ↓)	t_{CAH3}		10		ns
WR# setup time	t_{WCS}		0		ns
WR# hold time (from UCAS#/LCAS# ↓)	t_{WCH}		20		ns
Data output setup time	t_{D1}		0		ns
Data output hold time	t_{D2}		10		ns

Caution These ratings are applied only when a device operates within the recommended operating condition range and the operating ambient temperature is kept constant.
If the power supply voltage or operating ambient temperature changes during DRAM access, the above ratings are not applied.

(6) EDO-type DRAM write parameter (2/2)



Notes 1. In 32-bit mode: Applied to MRAS (0:1)# pins
In 16-bit mode: Applied to UUCAS#/MRAS3#, ULCAS#/MRAS2#, and MRAS (0:1)# pins

2. In 32-bit mode: Applied to UUCAS#/MRAS3#, ULCAS#MRAS2#, UCAS#, and LCAS# pins
In 16-bit mode: Applied to UCAS# and LCAS# pins

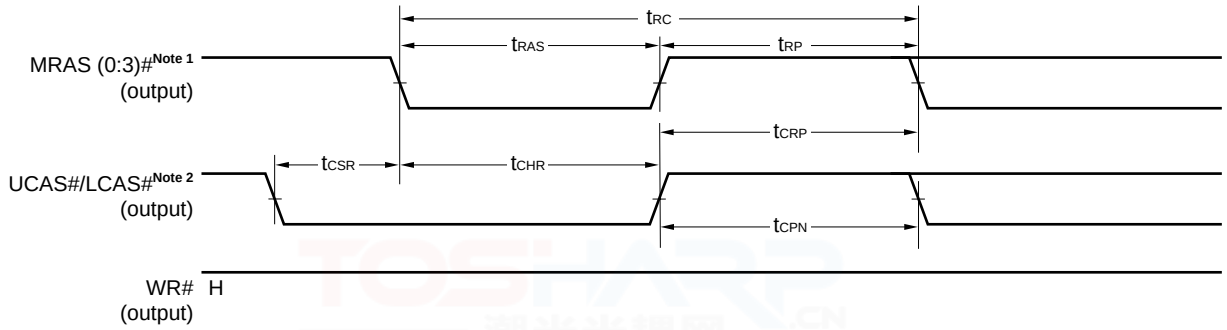
3. In 32-bit mode: Applied to DATA (16:31)/GPIO (16:31) and DATA (0:15) pins
In 16-bit mode: Applied to DATA (0:15) pins

(7) DRAM refresh parameter

The target DRAM is the μPD42S161615L-A60, 42S18165L-A60, 42S64165G5-A50, 42S64165G5-A60, 42S65165G5-A50, or 42S65165G5-A60.

(a) CAS-before-RAS refresh parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Read/write cycle time	t_{RC}		104		ns
MRAS (0:3)# pulse width	t_{RAS}		60		ns
MRAS (0:3)# precharge time	t_{RP}		30		ns
UCAS#/LCAS# setup time (to MRAS (0:3)# ↓)	t_{CSR}		5		ns
UCAS#/LCAS# hold time (from MRAS (0:3)# ↓)	t_{CHR}		10		ns
MRAS (0:3)# precharge time from UCAS#/LCAS# ↑	t_{CRP}		5		ns
UCAS#/LCAS# precharge time	t_{CPN}		10		ns



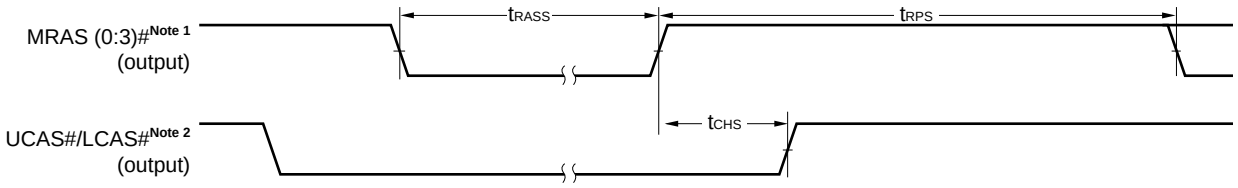
Notes 1. In 32-bit mode: Applied to MRAS (0:1)# pins
In 16-bit mode: Applied to UUCAS#/MRAS3#, ULCAS#/MRAS2#, and MRAS (0:1)# pins

2. In 32-bit mode: Applied to UUCAS#/MRAS3#, ULCAS#MRAS2#, UCAS#, and LCAS# pins
In 16-bit mode: Applied to UCAS# and LCAS# pins

(b) CAS-before-RAS self-refresh parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
MRAS (0:3)# pulse width[Note]	t_{RASS}		100		μs
MRAS (0:3)# precharge time	t_{RPS}		110		ns
UCAS#/LCAS# hold time	t_{CHS}		–50		ns

Note The CAS-before-RAS self-refresh parameter is valid when t_{RASS} exceeds 100 μs.



Notes 1. In 32-bit mode: Applied to MRAS (0:1)# pins
In 16-bit mode: Applied to UUCAS#/MRAS3#, ULCAS#/MRAS2#, and MRAS (0:1)# pins
2. In 32-bit mode: Applied to UUCAS#/MRAS3#, ULCAS#MRAS2#, UCAS#, and LCAS# pins
In 16-bit mode: Applied to UCAS# and LCAS# pins

(8) Normal ROM parameter (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data access time (from address)[Note]	t_{ACC}		T × N – 19		ns
Data access time (from ROMCS (0:3)# ↓)[Note]	t_{CE}		T × N – 19		ns
Data access time (from RD#↓)[Note]	t_{OE}		T × (N – 1) – 29		ns
Data input setup time	t_{DS}		0		ns
Data input hold time	t_{DH}		5		ns

Note The value of N is set by using the WROMA (0:2) bits of the BCUSPEEDREG register.
The value of T is set by using the CLKSEL (0:2) signals (TxD/CLKSEL2, RTS#/CLKSEL1, and DTR#/CLKSEL0 pins).

CLKSEL2 Signal	CLKSEL1 Signal	CLKSEL0 Signal	T (ns)
1	1	1	RFU
1	1	0	35
1	0	1	33
1	0	0	30
0	1	1	33
0	1	0	30
0	0	1	33
0	0	0	38

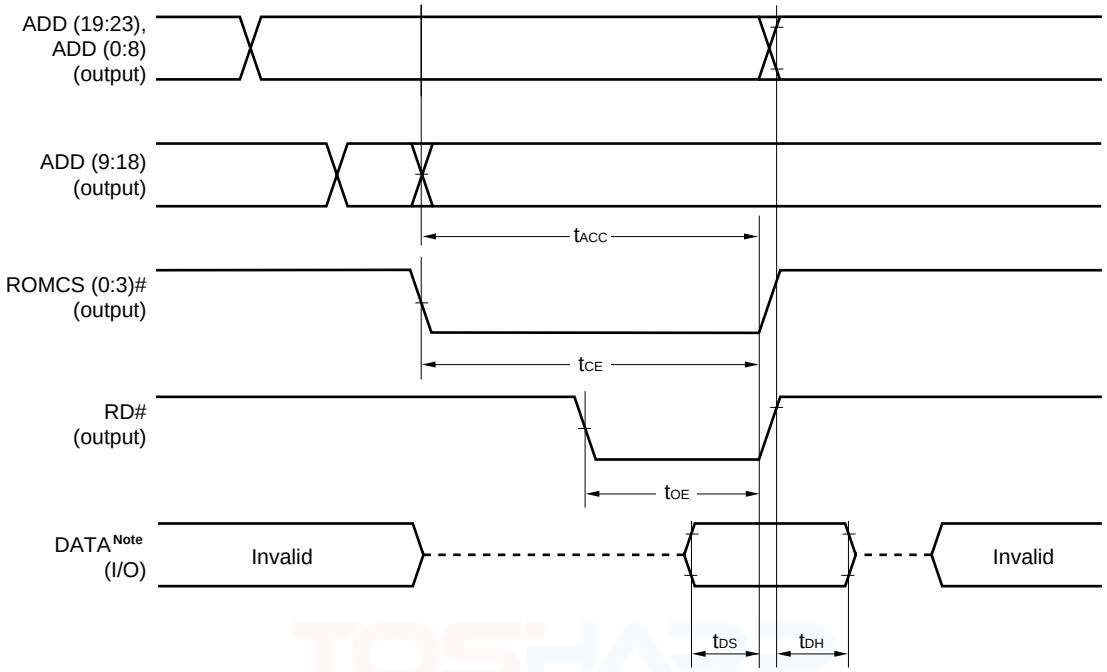
WROMA2 Bit	WROMA1 Bit	WROMA0 Bit	N (TClock)
0	0	0	9
0	0	1	8
0	1	0	7
0	1	1	6
1	0	0	5
1	0	1	4
1	1	0	3
1	1	1	2

Remarks 1. Do not set CLKSEL (2:0) signal = 111.

2. Do not set CLKSEL (2:0) signal = 110, 101 with 131 MHz model.

(8) Normal ROM parameter (2/2)

When WROMA (0:2) bits = 111



Note In 32-bit mode: Applied to DATA (16:31)/GPIO (16:31) and DATA (0:15) pins
In 16-bit mode: Applied to DATA (0:15) pins

Remark The broken lines indicate high impedance.

(9) Page ROM parameter (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data access time (from address)Note	t_{ACC1}		T × N – 19		ns
	t_{ACC2}		T × M – 18		ns
Data access time (from ROMCS (0:3)# ↓)Note	t_{CE}		T × N – 19		ns
Data access time (from RD#↓)Note	t_{OE}		T × (N – 1) – 29		ns
Data input setup time	t_{DS}		0		ns
Data input hold time	t_{DH}		5		ns

Note The value of N is set by using the WROMA (0:2) bits of the BCUSPEEDREG register.
The value of M is set by using the WPROM (0:1) bits of the BCUSPEEDREG register.
The value of T is set by using the CLKSEL (0:2) signals (TxD/CLKSEL2, RTS#/CLKSEL1, and DTR#/CLKSEL0 pins).

CLKSEL 2 Signal	CLKSEL 1 Signal	CLKSEL 0 Signal	T (ns)
1	1	1	RFU
1	1	0	35
1	0	1	33
1	0	0	30
0	1	1	33
0	1	0	30
0	0	1	33
0	0	0	38

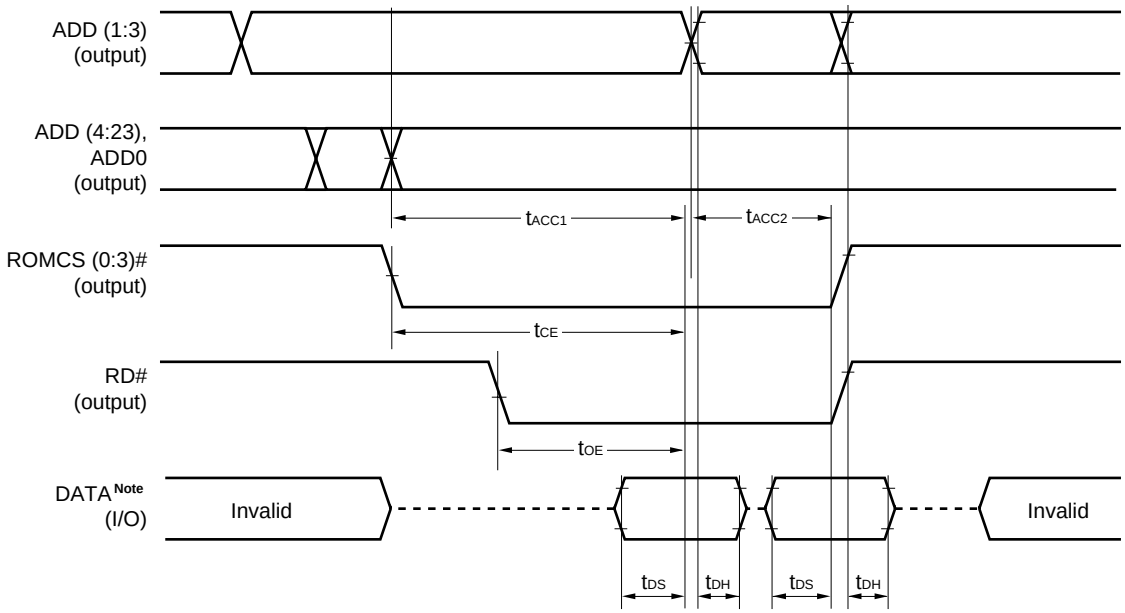
WROMA 2 Bit	WROMA 1 Bit	WROMA 0 Bit	N (TClock)
0	0	0	9
0	0	1	8
0	1	0	7
0	1	1	6
1	0	0	5
1	0	1	4
1	1	0	3
1	1	1	2

WPROM 1 Bit	WPROM 0 Bit	M (TClock)
0	0	3
0	1	2
1	0	1
1	1	—

Remarks 1. Do not set CLKSEL (2:0) signal = 111.

2. Do not set CLKSEL (2:0) signal = 110, 101 with 131 MHz model.

(9) Page ROM parameter (2/2)

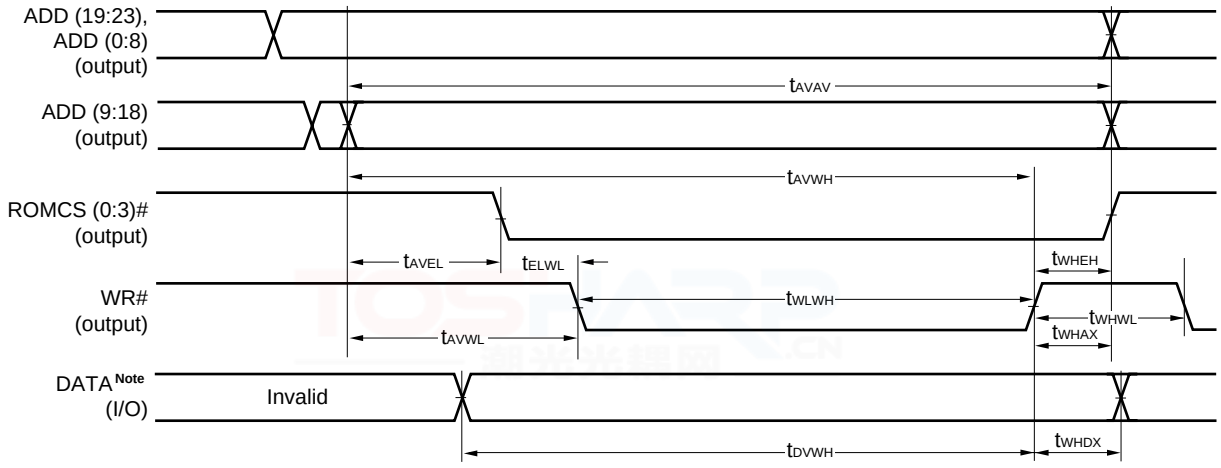


Note In 32-bit mode: Applied to DATA (16:31)/GPIO (16:31) and DATA (0:15) pins
In 16-bit mode: Applied to DATA (0:15) pins

Remark The broken lines indicate high impedance.

(10) Flash memory mode write parameter

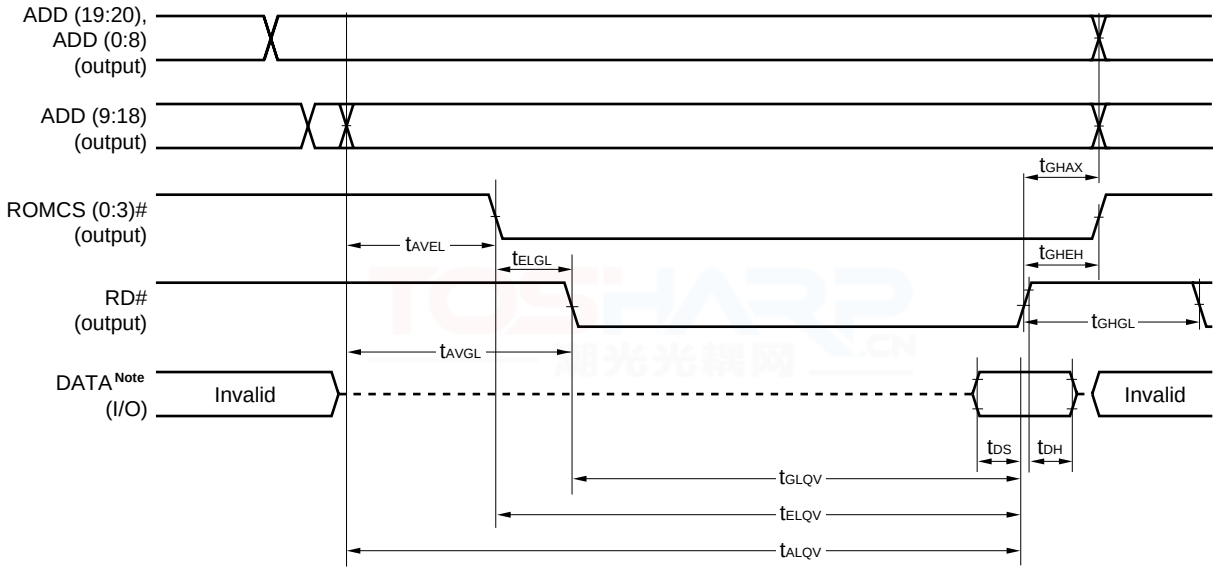
Parameter	Symbol	Condition	MIN.	MAX.	Unit
Write cycle time	t_{AVAV}		150		ns
Address setup time (to WR# ↑)	t_{AVWH}		75		ns
Address setup time (to ROMCS (0:3)# ↓)	t_{AVEL}		0		ns
ROMCS (0:3)# setup time (to WR#↓)	t_{ELWL}		10		ns
WR# low-level width	t_{WLWH}		75		ns
ROMCS (0:3)# hold time (from WR# ↑)	t_{WHEH}		10		ns
Address hold time (from WR# ↑)	t_{WHAX}		10		ns
WR# high-level width	t_{WHWL}		75		ns
Address setup time (to WR# ↓)	t_{AVWL}		25		ns
Data output setup time (to WR# ↑)	t_{DVWH}		75		ns
Data output hold time (from WR# ↑)	t_{WHDX}		10		ns



Note In 32-bit mode: Applied to DATA (16:31)/GPIO (16:31) and DATA (0:15) pins
In 16-bit mode: Applied to DATA (0:15) pins

(11) Flash memory mode read parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data output delay time from address	t_{AVQV}		180		ns
Data output delay time from ROMCS (0:3)#	t_{ELQV}		180		ns
Address setup time (to ROMCS (0:3)# ↓)	t_{AVEL}		0		ns
Data output delay time from RD# ↓	t_{GLQV}		80		ns
Address setup time (to RD# ↓)	t_{AVGL}		0		ns
ROMCS (0:3)# hold time (from RD# ↑)	t_{GHEH}		10		ns
Address hold time (from RD# ↑)	t_{GHAX}		10		ns
RD# high-level width	t_{GHGL}		75		ns
Data input setup time	t_{DS}		0		ns
Data input hold time	t_{DH}		5		ns
ROMCS (0:3)# setup time (to RD# ↓)	t_{ELGL}		10		ns



Note In 32-bit mode: Applied to DATA (16:31)/GPIO (16:31) and DATA (0:15) pins
In 16-bit mode: Applied to DATA (0:15) pins

Remark The broken lines indicate high impedance.

(12) System bus parameter (IOCHRDY) (1/3)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
BUSCLK high-level width	t_{BCLKH1}	**Note 1**	45		ns
	t_{BCLKH2}	**Note 2**	10		ns
BUSCLK low-level width	t_{BCLKL1}	**Note 1**	45		ns
	t_{BCLKL2}	**Note 2**	10		ns
Address setup time (to BUSCLK)	t_{AVCK}		15		ns
Address setup time (to command signal ↓)Notes 3, 4	t_{AVCL}		T × N – 29		ns
Command signal setup time (to BUSCLK)Note 3	t_{CLCK}		15		ns
Command signal low-level widthNotes 3, 4	t_{CLCH}		2 × T × N – 29		ns
Address hold time (from command signal ↑)Note 3	t_{CHAV}		25		ns
Command signal recovery timeNotes 3, 4	t_{CHCL}		T × (N + 1) – 29		ns
IOCHRDY sampling timeNote 4	t_{CLR}		0	T × N – 44	ns
Command signal ↑ delay time from IOCHRDY ↑Notes 3, 4	t_{RHCH}		T × N	2 × T × N + 29	ns
IOCHRDY hold time (from command signal ↑)Note 3	t_{CHRL}		0		ns
Data output setup time (to command signal ↓)Note 3	t_{DVCL}		0		ns
Data output hold time (from command signal ↑)Note 3	t_{CHDV}		25		ns
MEMCS16#/IOCS16# sampling start timeNote 4	t_{AVSV1}		2 × T × N – 44		ns
MEMCS16#/IOCS16# hold time (from command signal ↓)Note 3	t_{CHSV}		0		ns
Data input setup time	t_{DS}		0		ns
Data input hold time	t_{DH}		5		ns

Notes 1. Applied to BUSCLK pin when BSEL bit of BCUCNTREG3 register is 0.

2. Applied to BUSCLK pin when BSEL bit of BCUCNTREG3 register is 1.

3. With the VR4121, the MEMW#, MEMR#, IOW#, and IOR# signals are called the command signals for the system bus interface.

4. The value of N is set by using the WISAA (0:2) bits of the BCUSPEEDREG register.
The value of T is set by using the CLKSEL (0:2) signals (TxD/CLKSEL2, RTS#/CLKSEL1, and DTR#/CLKSEL0 pins).

CLKSEL2 Signal	CLKSEL1 Signal	CLKSEL0 Signal	T (ns)
1	1	1	RFU
1	1	0	35
1	0	1	33
1	0	0	30
0	1	1	33
0	1	0	30
0	0	1	33
0	0	0	38

WISAA2 Bit	WISAA1 Bit	WISAA0 Bit	N (TClock)
0	0	0	8
0	0	1	7
0	1	0	6
0	1	1	5
1Note	0Note	0Note	4
1Note	0Note	1Note	3
1	1	0	—
1	1	1	—

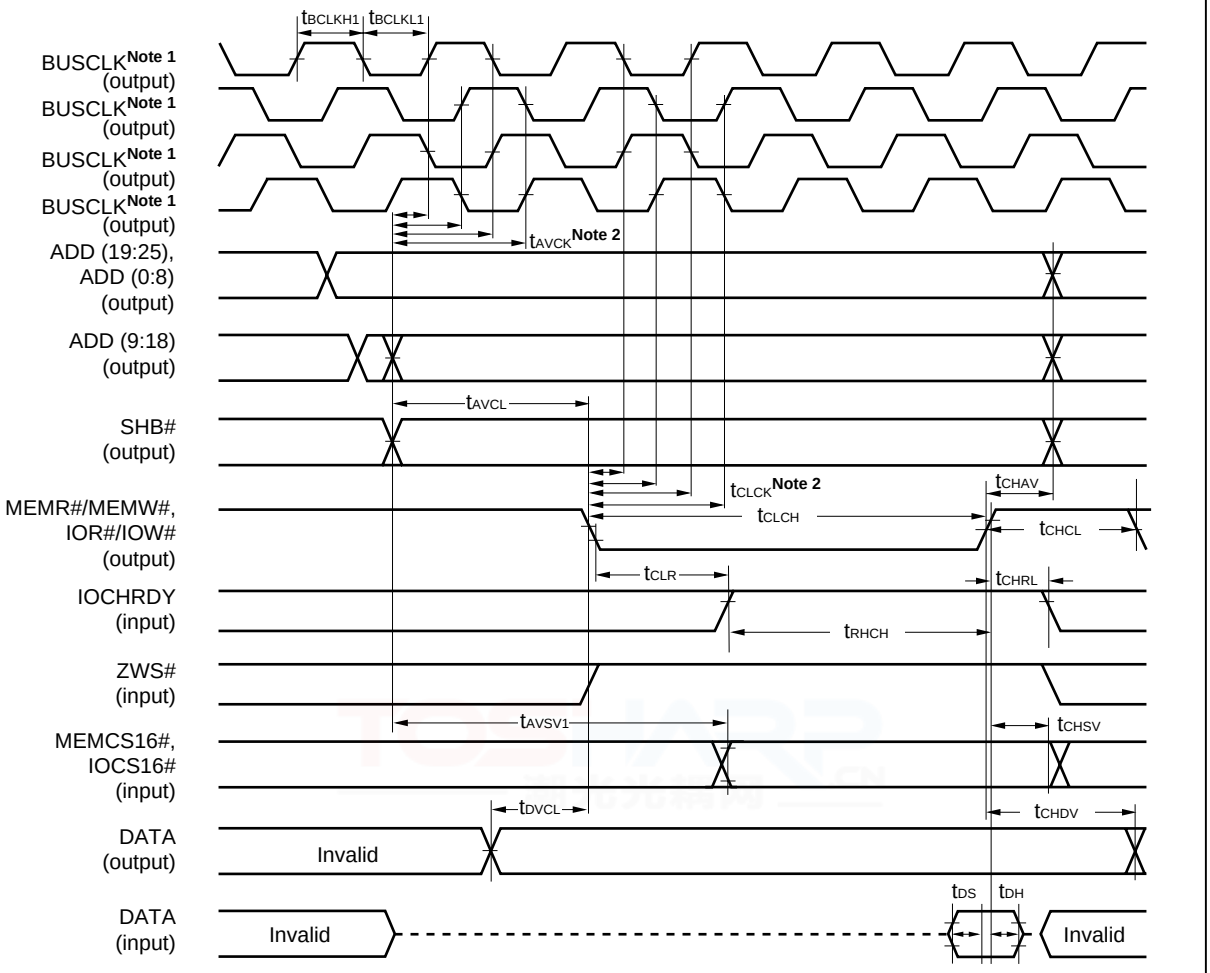
Remarks 1. Do not set CLKSEL (2:0) signal = 111.

2. Do not set CLKSEL (2:0) signal = 110, 101 with 131 MHz model.

Note If the WISAA (0:2) bits are set to 100 or high when BSEL bit of BCUCNTREG3 register is 0, the AC characteristics of t_{AVCK} and t_{CLCK} are not guaranteed.

(12) System bus parameter (IOCHRDY) (2/3)

When WISAA (0:2) bits = 010, BSEL bit = 0



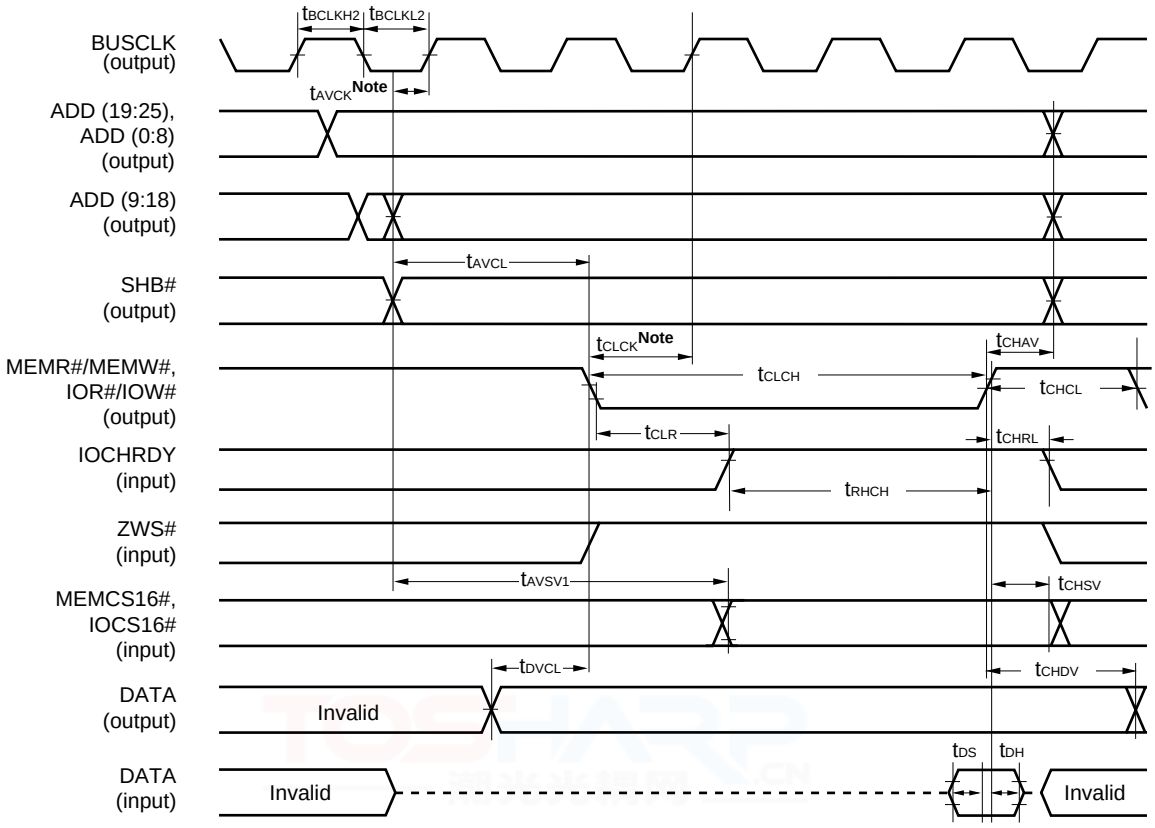
Notes 1. This indicates that there are four possible relationships between BUSCLK signal and other system bus interface signals.

2. This indicates the minimum setup time to the BUSCLK signal rising or falling edge.

Remark The broken lines indicate high impedance.

(12) System bus parameter (IOCHRDY) (3/3)

When WISAA (0:2) bits = 010, BSEL bit = 1



Note This indicates the minimum setup time to the BUSCLK signal rising edge.

Remark The broken lines indicate high impedance.

(13) System bus parameter (ZWS#) (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Address setup time (to BUSCLK)	t_{AVCK}		15		ns
Address setup time (to command signal ↓)[Notes 1, 2]	t_{AVCL}		T × N – 29		ns
Command signal setup time (to BUSCLK)[Note 1]	t_{CLCK}		15		ns
Command signal low-level width[Notes 1, 2]	t_{CLCH}		T × N – 19		ns
Address hold time (from command signal ↑)[Note 1]	t_{CHAV}		25		ns
Command signal recovery time[Notes 1, 2]	t_{CHCL}		T × (N + 1) – 29		ns
ZWS# ↓ delay time from command signal ↓[Notes 1, 2]	t_{CLZL}			T × (N – 1) – 20	ns
ZWS# hold time (from command signal ↑)[Note 1]	t_{CHZH}		0		ns
Data output setup time (to command signal ↓)[Note 1]	t_{DVCL}		0		ns
Data output hold time (from command signal ↑)[Note 1]	t_{CHDV}		25		ns
MEMCS16#/IOCS16# sampling start time[Note 2]	t_{AVSV2}		2 × T × (N – 1) – 44		ns
MEMCS16#/IOCS16# hold time (from command signal ↑)[Note 1]	t_{CHSV}		0		ns
Data input setup time	t_{DS}		0		ns
Data input hold time	t_{DH}		5		ns

Notes 1. With the VR4121, the MEMW#, MEMR#, IOW#, and IOR# signals are called the command signals for the system bus interface.

2. The value of N is set by using the WISAA (0:2) bits of the BCUSPEEDREG register.
The value of T is set by using the CLKSEL (0:2) signals (TxD/CLKSEL2, RTS#/CLKSEL1, and DTR#/CLKSEL0 pins).

CLKSEL2 Signal	CLKSEL1 Signal	CLKSEL0 Signal	T (ns)
1	1	1	RFU
1	1	0	35
1	0	1	33
1	0	0	30
0	1	1	33
0	1	0	30
0	0	1	33
0	0	0	38

WISAA2 Bit	WISAA1 Bit	WISAA0 Bit	N (TClock)
0	0	0	8
0	0	1	7
0	1	0	6
0	1	1	5
1[Note]	0[Note]	0[Note]	4
1[Note]	0[Note]	1[Note]	3
1	1	0	—
1	1	1	—

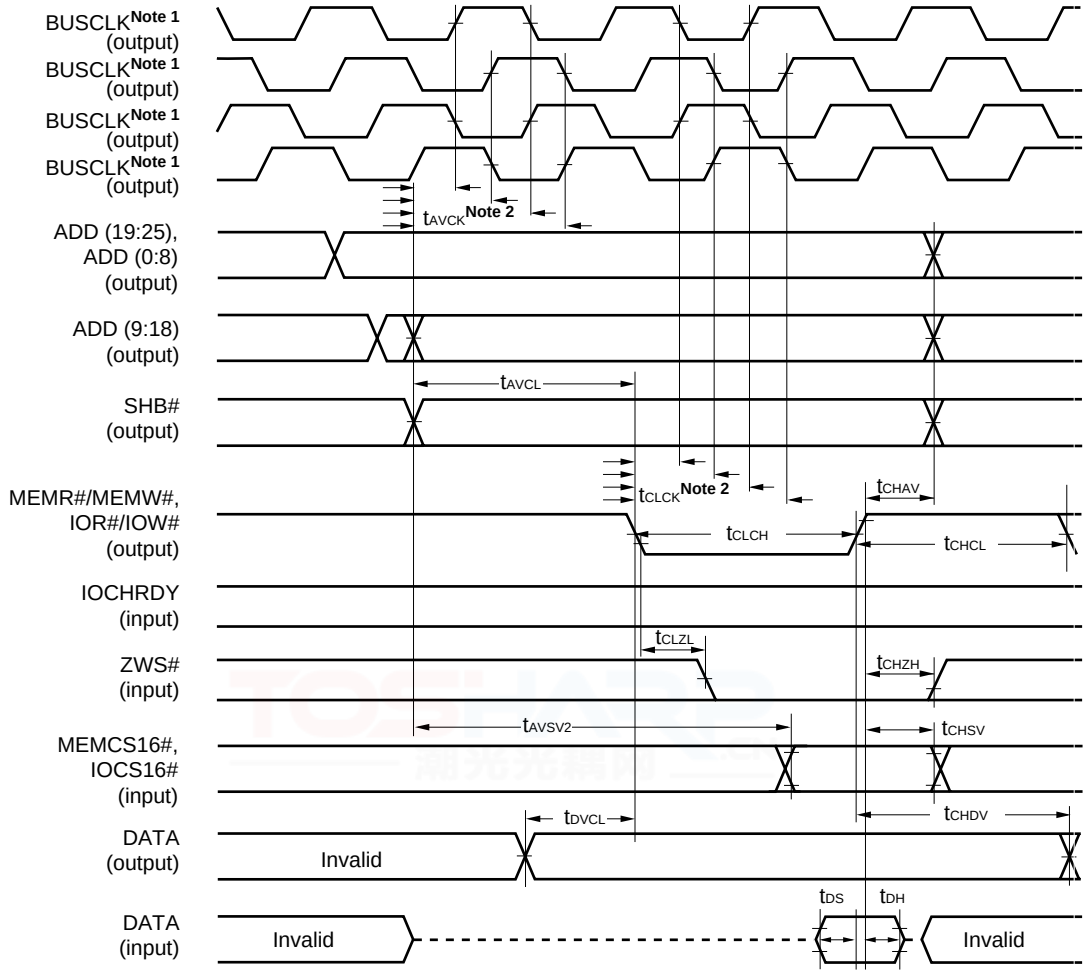
Remarks 1. Do not set CLKSEL (2:0) signal = 111.

2. Do not set CLKSEL (2:0) signal = 110, 101 with 131 MHz model.

Note If the WISAA (0:2) bits are set to 100 or high, the AC characteristics of t_{CLCK} and t_{AVCK} are not guaranteed.

(13) System bus parameter (ZWS#) (2/2)

When WISAA (0:2) bits = 101, BSEL bit = 0



Notes 1. This indicates that there are four possible relationships between BUSCLK signal and other system bus interface signals.

2. This indicates the minimum setup time to the BUSCLK signal rising or falling edge.

Remark The broken lines indicate high impedance.

(14) High-speed system bus parameter (IOCHRDY) (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Address setup time (to command signal ↓)Notes 1, 2	t_{AVCL}		T × N – 29		ns
Command signal low-level widthNotes 1, 2	t_{CLCH}		T × (N + M) – 29		ns
Address hold time (from command signal ↑)Note 1	t_{CHAV}		25		ns
Command signal recovery timeNotes 1, 2	t_{CHCL}		T × (N + 1) – 29		ns
IOCHRDY sampling start time	t_{CLR}		0		ns
Command signal ↑ delay time from IOCHRDY ↑Notes 1, 2	t_{RHCH}		T × M	T × (N + M) + 29	ns
IOCHRDY hold time (from command signal ↑)Note 1	t_{CHRL}		0		ns
Data output setup time (to command signal ↓)Note 1	t_{DVCL}		–15		ns
Data output hold time (from command signal ↑)Note 1	t_{CHDV}		25		ns
MEMCS16#/IOCS16# sampling start timeNote 2	t_{AVSV1}		2 × T × N – 44		ns
MEMCS16#/IOCS16# hold time (from command signal ↑)Note 1	t_{CHSV}		0		ns
Data input setup time	t_{DS}		0		ns
Data input hold time	t_{DH}		5		ns

Notes 1. With the VR4121, the MEMW# and MEMR# signals are called the command signals for the high-speed system bus interface.

2. The values of N and M are set by using the WLCD/M (0:2) bits of the BCUSPEEDREG register.
The value of T is set by using the CLKSEL (0:2) signals (TxD/CLKSEL2, RTS#/CLKSEL1, and DTR#/CLKSEL0 pins).

CLKSEL2 Signal	CLKSEL1 Signal	CLKSEL0 Signal	T (ns)
1	1	1	RFU
1	1	0	35
1	0	1	33
1	0	0	30
0	1	1	33
0	1	0	30
0	0	1	33
0	0	0	38

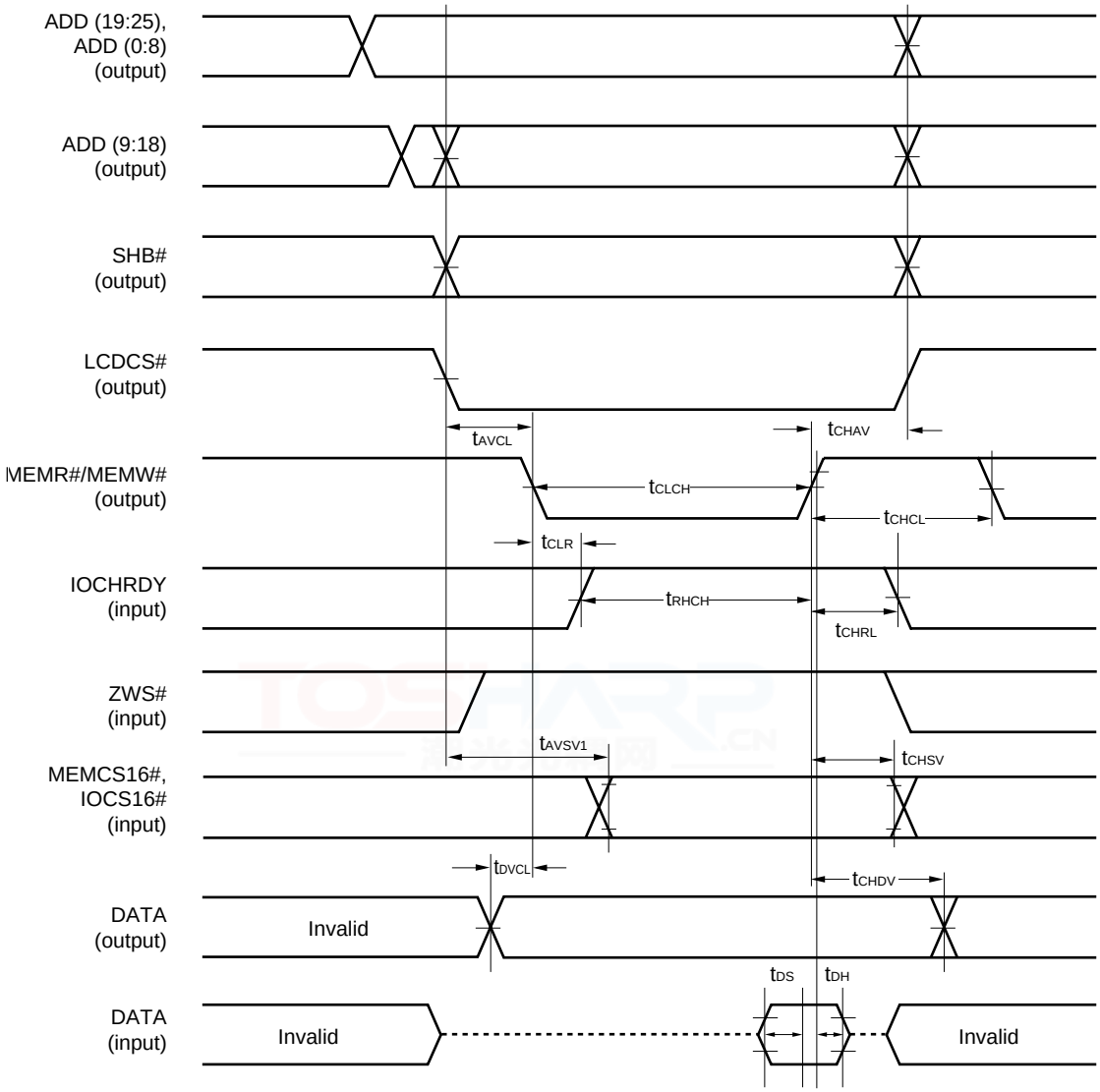
WLCD/M2 Bit	WLCD/M1 Bit	WLCD/M0 Bit	N (TClock)	M (TClock)
0	0	0	8	8
0	0	1	7	7
0	1	0	6	6
0	1	1	5	5
1	0	0	4	4
1	0	1	3	3
1	1	0	2	2
1	1	1	1	2

Remarks 1. Do not set CLKSEL (2:0) signal = 111.

2. Do not set CLKSEL (2:0) signal = 110, 101 with 131 MHz model.

(14) High-speed system bus parameter (IOCHRDY) (2/2)

When WISAA (2:0) bits = 111



Remark The broken lines indicate high impedance.

(15) High-speed system bus parameter (ZWS#) (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Address setup time (to command signal ↓)Notes 1, 2	t_{AVCL}		T × N – 29		ns
Command signal low-level widthNotes 1, 2	t_{CLCH}		T × N – 19		ns
Address hold time (from command signal ↑)Note 1	t_{CHAV}		25		ns
Command signal recovery timeNotes 1, 2	t_{CHCL}		T × (N + 1) – 29		ns
ZWS# ↓ delay time from command signal ↓Notes 1, 2	t_{CLZL}			T × (N – 1) – 20	ns
ZWS# signal hold time (from command signal ↑)Note 1	t_{CHZH}		0		ns
Data output setup time (to command signal ↓)Note 1	t_{DVCL}		–15		ns
Data output hold time (from command signal ↑)Note 1	t_{CHDV}		25		ns
MEMCS16#/IOCS16# sampling start timeNote 2	t_{AVSV2}		2 × T × (N – 1) – 44		ns
MEMCS16#/IOCS16# hold time (from command signal ↑)Note 1	t_{CHSV}		0		ns
Data input setup time	t_{DS}		0		ns
Data input hold time	t_{DH}		5		ns

Notes 1. With the VR4121, the MEMW# and MEMR# signals are called the command signals for the high-speed system bus interface.

2. The value of N is set by using the WISAA (0:2) bits of the BCUSPEEDREG register.
The value of T is set by using the CLKSEL (0:2) signals (TxD/CLKSEL2, RTS#/CLKSEL1, and DTR#/CLKSEL0 pins).

CLKSEL2 Signal	CLKSEL1 Signal	CLKSEL0 Signal	T (ns)
1	1	1	RFU
1	1	0	35
1	0	1	33
1	0	0	30
0	1	1	33
0	1	0	30
0	0	1	33
0	0	0	38

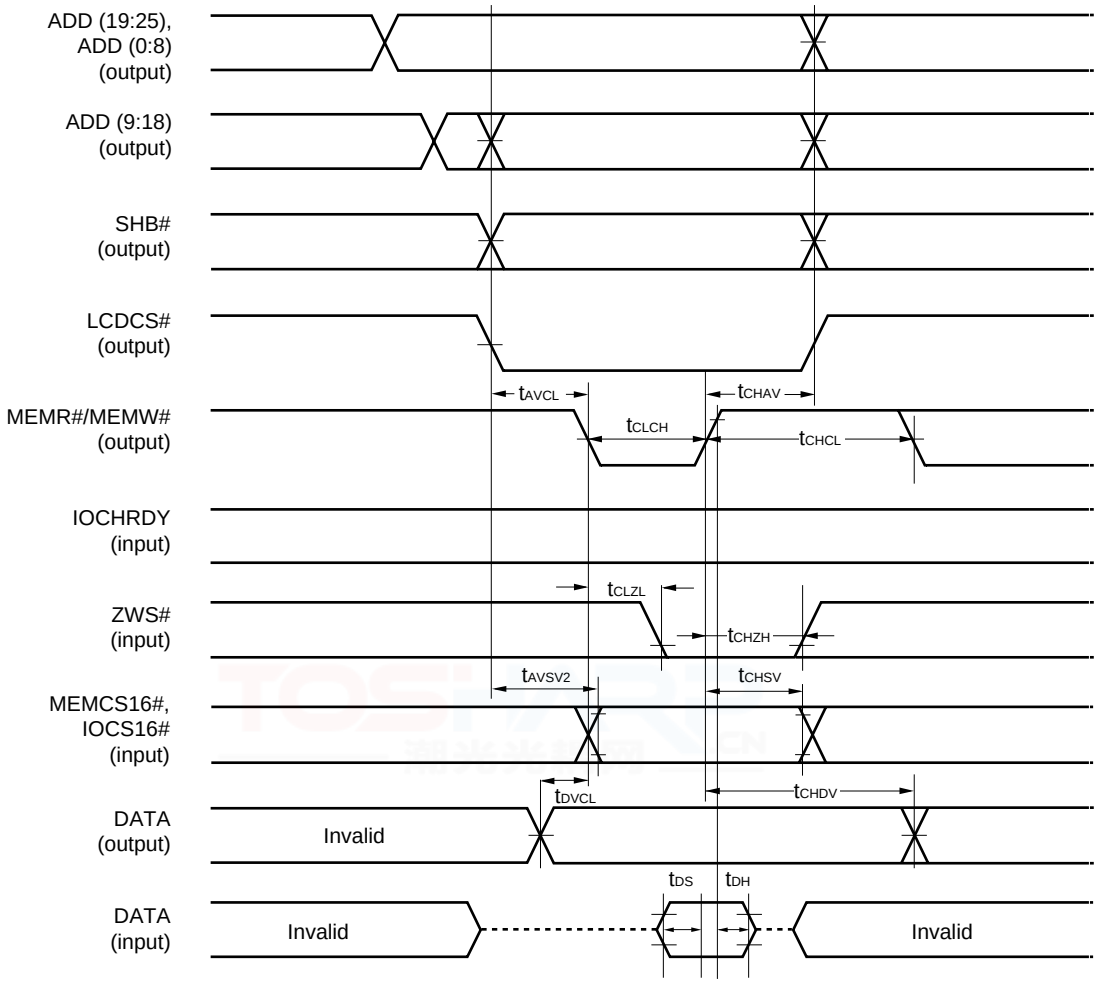
WISAA2 Bit	WISAA1 Bit	WISAA0 Bit	N (TClock)
0	0	0	8
0	0	1	7
0	1	0	6
0	1	1	5
1	0	0	4
1	0	1	3
1	1	0	2
1	1	1	1

Remarks 1. Do not set CLKSEL (2:0) signal = 111.

2. Do not set CLKSEL (2:0) signal = 110, 101 with 131 MHz model.

(15) High-speed system bus parameter (ZWS#) (2/2)

When WISAA (0:2) bits = 111



Remark The broken lines indicate high impedance.

(16) LCD interface parameter (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Address setup time (to command signal ↓)Note 1	t_{AS}		15		ns
Address hold time (from command signal ↑)Note 1	t_{AH}		0		ns
Command signal recovery timeNote 1	t_{RY}		30		ns
LCDRDY sampling start time	t_{CLR}		0		ns
Command signal delay time from LCDRDY ↑Notes 1, 2	t_{RHCH}		T × N	T × (N + 2) + 29	ns
LCDRDY hold time (from command signal ↑)Note 1	t_{RYZ}		0		ns
Data output setup time (to command signal ↑)Notes 1, 2	t_{DVCH}		T × (N + 2)		ns
Data output hold time (from command signal ↑)Note 1	t_{CHDV}		25		ns
Data input setup time (to command signal ↑)Note 1	t_{DS}		0		ns
Data input hold time (from command signal ↑)Note 1	t_{DH}		5		ns

Notes 1. With the VR4121, the RD# and WR# signals are called the command signals for the LCD interface.

2. The values of N is set by using the WLCD/M (0:1) bits of the BCUSPEEDREG register.
The value of T is set by using the CLKSEL (0:2) signals (TxD/CLKSEL2, RTS#/CLKSEL1, and DTR#/CLKSEL0 pins).

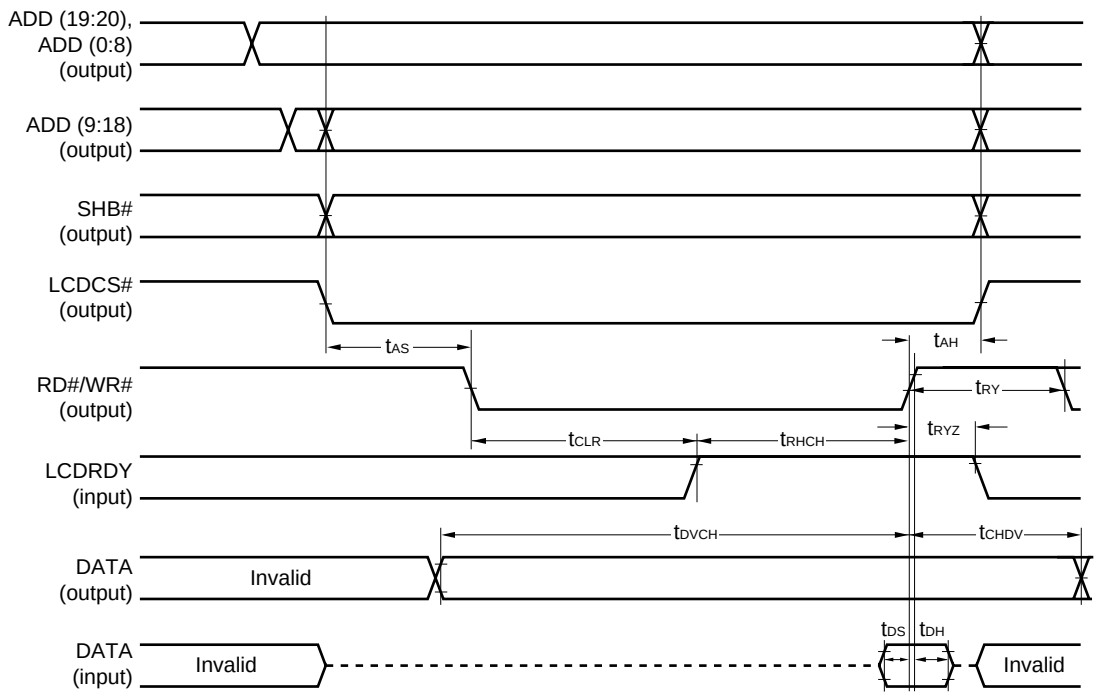
CLKSEL2 Signal	CLKSEL1 Signal	CLKSEL0 Signal	T (ns)
1	1	1	RFU
1	1	0	35
1	0	1	33
1	0	0	30
0	1	1	33
0	1	0	30
0	0	1	33
0	0	0	38

WLCD/M1 Bit	WLCD/M0 Bit	N (TClock)
0	0	8
0	1	6
1	0	4
1	1	2

Remarks 1. Do not set CLKSEL (2:0) signal = 111.

2. Do not set CLKSEL (2:0) signal = 110, 101 with 131 MHz model.

(16) LCD interface parameter (2/2)



Remark The broken lines indicate high impedance.

(17) Bus hold parameter (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
HLDRQ# input pulse width[Note]	t_{FHP}	In Fullspeed/Standby mode	5T		ns
Data floating delay time	t_{FOFF}	In Fullspeed/Standby mode	0		ns
Data valid delay time	t_{FON}	In Fullspeed/Standby mode	0		ns
HLDRQ# input pulse width[Note]	t_{SHP}	In Suspend mode	12T		ns
Data floating delay time	t_{SOFF}	In Suspend mode	0		ns
Data valid delay time	t_{SON}	In Suspend mode	0		ns
MRAS (0:3)# precharge time	t_{RPS}	In Suspend mode	110		ns
UCAS#/LCAS# setup time	t_{CSR}	In Suspend mode	5		ns

Note The value of T is set by using the CLKSEL (0:2) signals (TxD/CLKSEL2, RTS#/CLKSEL1, and DTR#/CLKSEL0 pins).

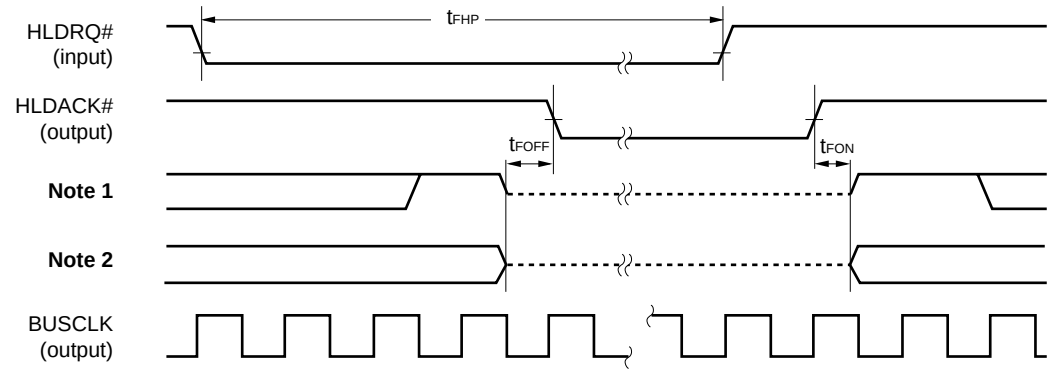
CLKSEL2 Signal	CLKSEL1 Signal	CLKSEL0 Signal	T (ns)
1	1	1	RFU
1	1	0	35
1	0	1	33
1	0	0	30
0	1	1	33
0	1	0	30
0	0	1	33
0	0	0	38

Remarks 1. Do not set CLKSEL (2:0) signal = 111.

2. Do not set CLKSEL (2:0) signal = 110, 101 with 131 MHz model.

(17) Bus hold parameter (2/2)

(a) Bus hold in Fullspeed/Standby mode

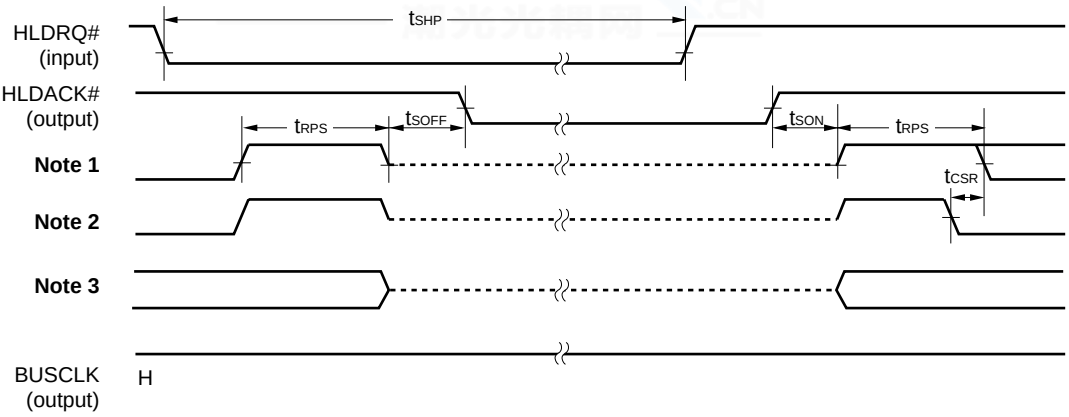


Notes 1. UUCAS#/MRAS3#, ULCAS#/MRAS2#, MRAS (0:1)#, UCAS#, LCAS# pins

2. SHB#, IOR#, IOW#, MEMR#, MEMW#, RD#, WR#, ADD (0:24), ADD25/SCLK, and DATA (0:15) pins, and DATA (16:31)/GPIO (16:31) pin in 32-bit mode

Remark The broken lines indicate high impedance.

(b) Bus hold in Suspend mode



Notes 1. In 32-bit mode: MRAS (0:1)# pins
In 16-bit mode: UUCAS#/MRAS3#, ULCAS#/MRAS2#, MRAS (0:1)# pins

2. In 32-bit mode: UUCAS#/MRAS3#, ULCAS#/MRAS2#, UCAS#, LCAS# pins
In 16-bit mode: UCAS#, LCAS# pins

3. SHB#, IOR#, IOW#, MEMR#, MEMW#, RD#, WR#, ADD (0:24), ADD25/SCLK, and DATA (0:15) pins, and DATA (16:31)/GPIO (16:31) pins in 32-bit mode

Remark The broken lines indicate high impedance.

(18) Keyboard Interface parameter (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
KSCAN (0:11) high-level width	t_{SCAN}		30 (K + 2) – 1	30.16 (K + 2) + 1	μs
Idle time (KSCAN (n+1) ↑ from KSCANn ↓)	t_{KWAIT}		30 (L + 1) – 1	30.16 (L + 1) + 1	μs
Key scan interval time	t_{KI}		30M – 1	30.16M + 1	μs
Key input setup time (to KSCANn ↑)	t_{KS}		30 (N + 1) – 1		μs
Key input hold time (from KSCANn ↑)	t_{KH}		0		μs

Notes 1. K: Sum of the values set to the T1CNT (0:4) bits and T2CNT (0:4) bits of the KIUWKS register

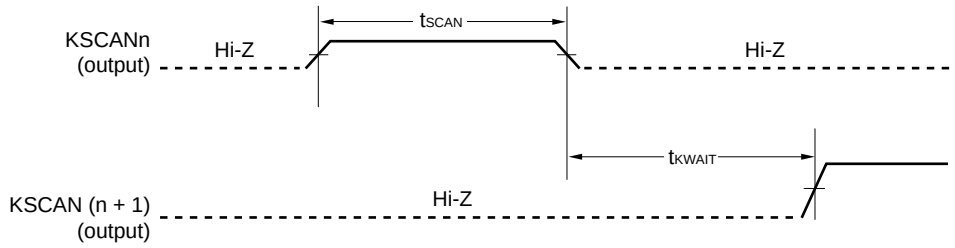
2. L: Value set to the T3CNT (0:4) bits of the KIUWKS register

3. M: Value set to KIUWKI register

4. N: Value set to the T1CNT (0:4) bits of the KIUWKS register

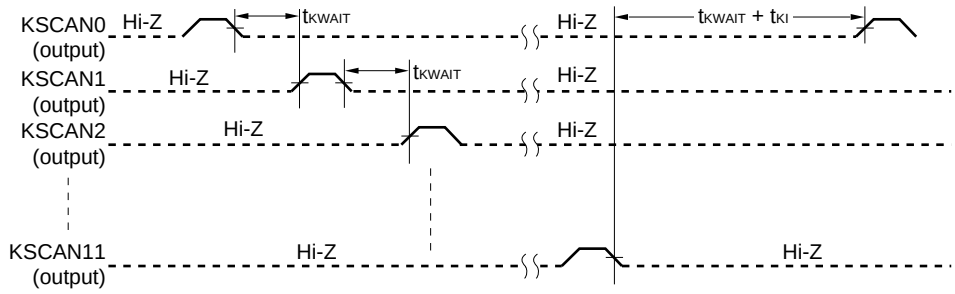
5. n = 0 to 11

(a) Keyboard scan parameter 1



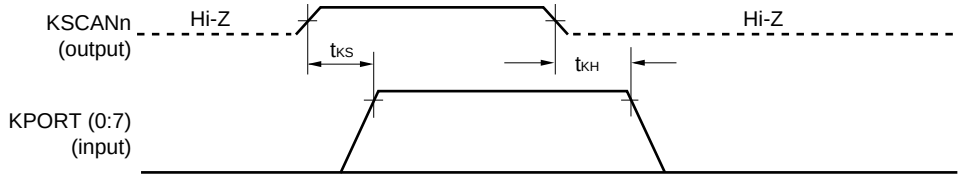
Remark n = 0 to 10

(b) Keyboard scan parameter 2



(18) Keyboard Interface parameter (2/2)

(c) Keyboard port parameter



Remark n = 0 to 11

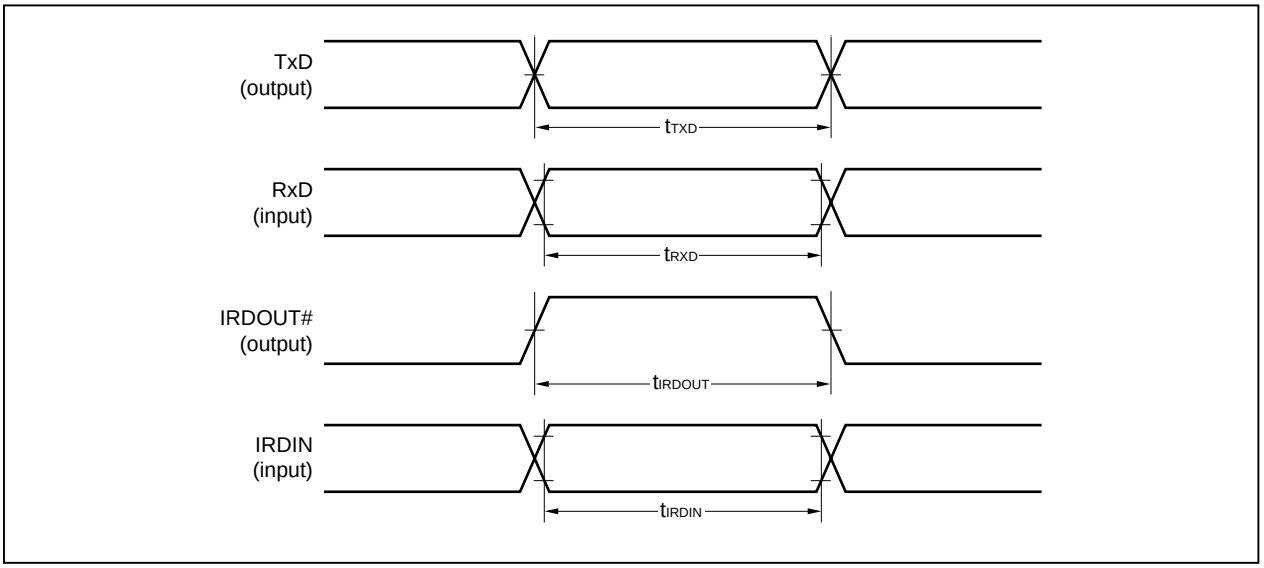
(19) Serial interface parameter (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
TxD output pulse width[Note]	t_{TXD}		N – 1	N + 1	μs
RxD input pulse width[Note]	t_{RXD}		(9/16) × N		μs
IRDOUT# high-level output pulse width[Note]	t_{IRDOUT}		(3/16) × N – 1	(3/16) × N + 1	μs
IRDIN input pulse width	t_{IRDIN}		1		μs

Note N: Data transfer rate per bit, which is determined by the divisor of the baud-rate generator that is set with the SIUDLL and SIUDLM registers.

Baud Rate (bps)	SIUDLM, SIUDLL Resister	N (μs)
50	23,040	20,000
75	15,360	13,333
110	10,473	9,091
134.5	8,565	7,435
150	7,680	6,667
300	3,840	3,333
600	1,920	1,667
1,200	920	833
1,800	640	556
2,000	573	500
2,400	480	417
3,600	320	278
4,800	240	208
7,200	160	139
9,600	120	104
19,200	60	52.1
38,400	30	26.0
56,000	21	17.9
128,000	9	7.81
144,000	8	6.94
192,000	6	5.21
230,400	5	4.34
288,000	4	3.47
384,000	3	2.60
576,000	2	1.74
1,152,000	1	0.868

(19) Serial interface parameter (2/2)

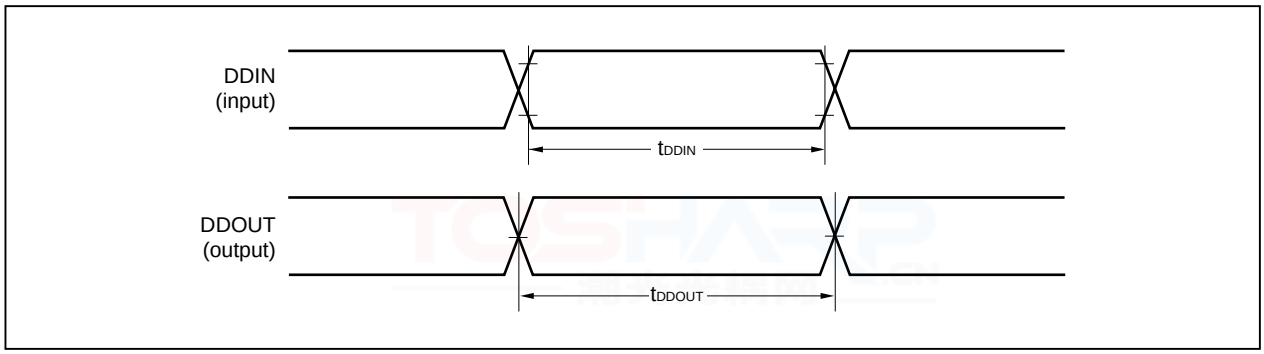


(20) Debug serial interface parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
DDOUT output pulse width[Note]	t_{DDOUT}		N – 1	N + 1	μs
DDIN input pulse width[Note]	t_{DDIN}		(9/16) × N		μs

Note N: Transfer rate of baud rate per bit set to the BPR0 bits of the BPRM0REG register.

BPR0 (2:0) Bits	Baud Rate (bps)	N (μs)
111	115,200	8.68
110	57,600	17.36
101	38,400	26.04
100	19,200	52.03
011	9,600	104.16
010	4,800	208.33
001	2,400	416.66
000	1,200	833.33



(21) HSP interface parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
SDO output delay time[Note 1]	t_{SDOD}			15	ns
SDI setup time[Note 2]	t_{SDIS}		25		ns
SDI hold time[Note 2]	t_{SDIH}		0		ns
FS setup time[Note 2]	t_{FSIS}		20		ns
FS hold time[Note 2]	t_{FSIH}		0		ns

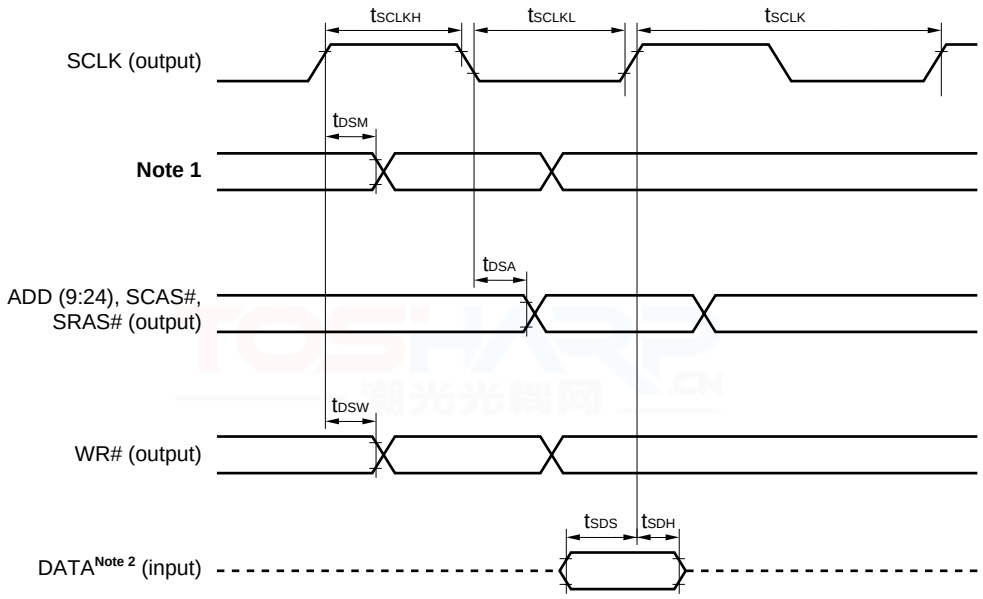
Notes 1. The reference clock of this parameter is the rising edge of HSPSCLK signal.

2. The reference clock of this parameter is the falling edge of HSPSCLK signal.

(22) SDRAM interface parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
SCLK clock cycle	t_{SCLK}		13.7		ns
SCLK high-level width	t_{SCLKH}		3.5		ns
SCLK low-level width	t_{SCLKL}		3.5		ns
Data output delay time (from SCLK ↑)	t_{DSM}		1.1	10.7	ns
Address output delay time (from SCLK ↓)	t_{DSA}		–5.8	17.6	ns
WR# output delay time (from SCLK ↑)	t_{DSW}		1.1	24.5	ns
Data input setup time	t_{SDS}	**Note**	6.2		ns
Data input hold time	t_{SDH}	**Note**	2.9		ns

Note DATA (0:15) pins and DATA (16:31)/GPIO (16:31) pins in 32-bit mode



Notes 1. MRAS (0:1)#, ROMCS (2:3)#, UUCAS#/MRAS3#, ULCAS#/MRAS2#, UCAS#, LCAS#, CKE, and DATA (0:15) pins, and DATA (16:31)/GPIO (16:31) pins in 32-bit mode

2. DATA (0:15) pins, and DATA (16:31)/GPIO (16:31) pins in 32-bit mode

Remark The broken lines indicate high impedance.

A/D Converter Characteristics (131 MHz model: T_A = –10 to +70°C, V_{DD2} = 2.3 to 2.7 V, V_{DD3} = 3.0 to 3.45 V
168 MHz model: T_A = –10 to +70°C, V_{DD2} = 2.6 to 2.7 V, V_{DD3} = 3.0 to 3.45 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Resolution			10			bit
Zero-scale error Notes 1, 2	ZSE		0	±4.0		LSB
Full-scale error Notes 1, 2	RSE		0	±5.0		LSB
Integral linearity error Notes 1, 2	INL		0	±3.0		LSB
Differential linearity error Notes 1, 2	DNL		0	±3.0		LSB
Analog input voltage Notes 1, 3	VIAN		–0.3		AV_{DD} + 0.3	V

Notes 1. Applied to TPX (0:1), TPY (0:1), ADIN (0:2), and AUDIOIN pins.
2. Quantization error is excluded.
3. AV_{DD} is a voltage on the AV_{DD} pin that is V_{DD} dedicated to the A/D converter.

D/A Converter Characteristics (131 MHz model: T_A = –10 to +70°C, V_{DD2} = 2.3 to 2.7 V, V_{DD3} = 3.0 to 3.45 V
168 MHz model: T_A = –10 to +70°C, V_{DD2} = 2.6 to 2.7 V, V_{DD3} = 3.0 to 3.45 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Resolution			10			bit
Integral linearity error Notes 1, 2	INL		0	±3.0		LSB
Differential linearity error Notes 1, 2	DNL		0	±3.0		LSB

Notes 1. Applied to AUDIOOUT pin.
2. Quantization error is excluded.

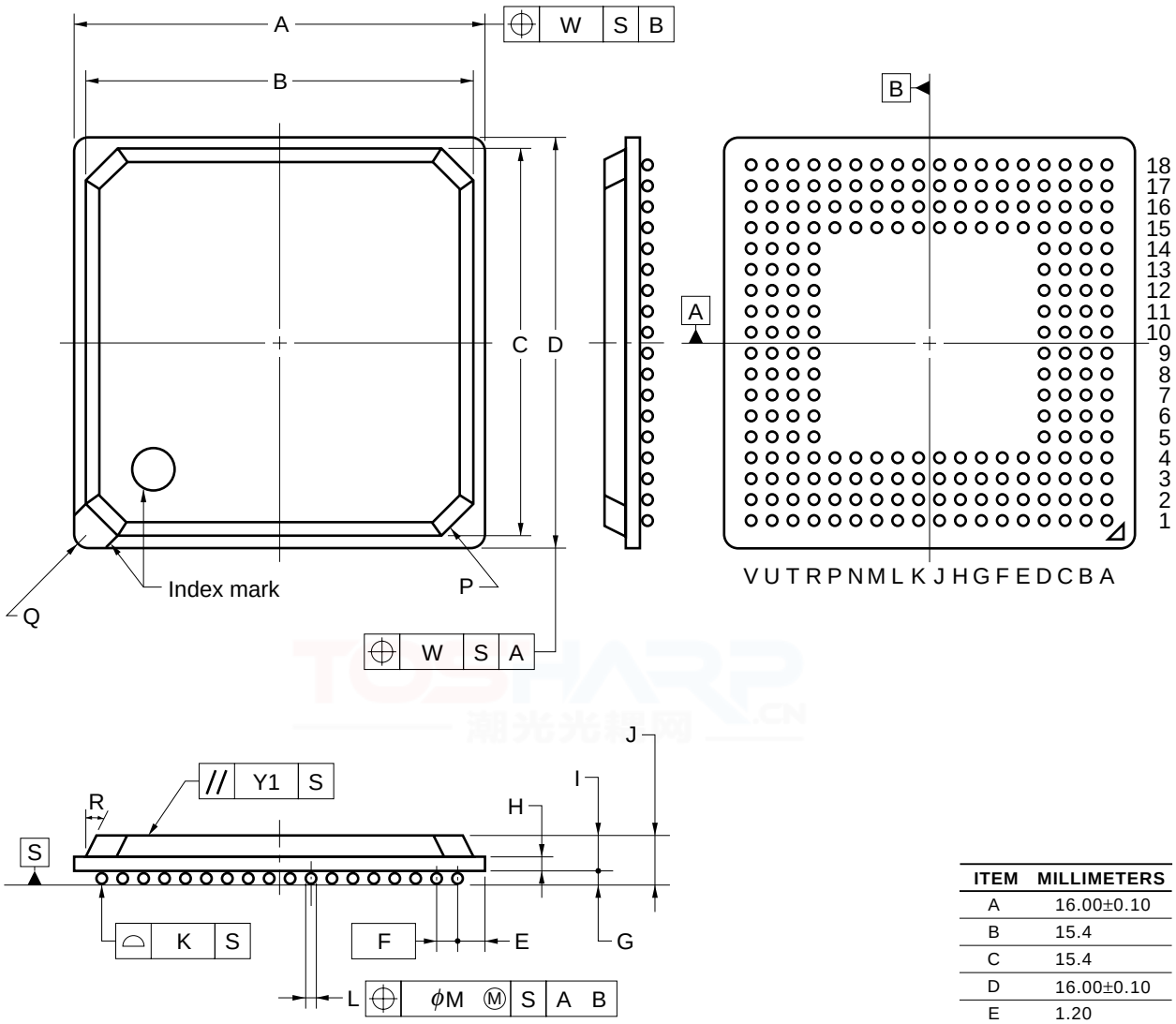
Load Coefficient (Delay Time per Load Capacitance)

Parameter	Symbol	Condition	Rating		Unit
			MIN.	MAX.	
Load coefficient	CLD			5	ns/20 pF

Caution Because NEC confirmed the characteristics by simulation at the design phase, screening on shipment is omitted.

3. PACKAGE DRAWING

224-PIN PLASTIC FBGA (16x16)



ITEM	MILLIMETERS
A	16.00±0.10
B	15.4
C	15.4
D	16.00±0.10
E	1.20
F	0.8 (T.P.)
G	0.35±0.1
H	0.36
I	0.96
J	1.31±0.15
K	0.10
L	$\phi 0.50^{+0.05}_{-0.10}$
M	0.08
P	C1.0
Q	R0.3
R	25°
W	0.20
Y1	0.20

S224S1-80-3C-2

4. RECOMMENDED SOLERING CONDITIONS

The μPD30121 should be soldered and mounted under the following recommended conditions.

For details of recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Table 4-1. Surface Mounting Type Soldering Conditions

μPD30121F1-131-GA1: 224-pin plastic FBGA (16 × 16)
μPD30121F1-168-GA1: 224-pin plastic FBGA (16 × 16)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 230°C, Time: 30 seconds max. (at 210°C or higher), Count: 2 times max., Exposure limit: 3 days[Note] (after that, prebake at 125°C for 10 to 72 hours.)	IR30-103-2
VPS	Package peak temperature: 215°C, Time: 25 to 40 seconds (at 200°C or higher), Count: 2 times max. , Exposure limit: 3 days[Note] (after that, prebake at 125°C for 10 to 72 hours.)	VP15-103-2
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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Reference document Electrical Characteristics for Microcomputer (IEI-601)[Note]

Note This document number is that of the Japanese version.

The documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

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